Modeling and Simulation of the C-V Characteristic of AlGaN-based UVC LEDs

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Introduction

UVC LEDs are complex heterostructure devices, therefore device-level characterization, such as L-I or I-V measurements, are often uncapable of providing information on the physical processes or on the physical features related to specific device layers. With this work, we propose a novel methodology to properly model the free charge profile, as well as specific non-idealities, of wide-bandgap heterostructure devices based on conventional C-V measurements and TCAD simulations.

Experimental Procedures

The devices under investigation are far-UVC LEDs grown by metalorganic vapor phase epitaxy (MOVPE) on high temperature annealed (HTA) epitaxially laterally grown (ELO) AlN/sapphire substrates (more details on the fabrication can be found in [1]). The LEDs feature three quantum-wells, two emitting at 233 nm and one at 250 nm. The devices have been characterized at room temperature by means of C-V measurements. Experimental data has been modeled by leveraging numerical simulations carried out through the Sentaurus suite (by Synopsys), previously adopted for the simulation of the forward leakage current in similar devices [2].

Results and Discussion

Gradual improvements in the definition of the simulations framework allowed us to match the experimental trends (Figure 1) and to evaluate the effect of specific non-idealities on the capacitance-voltage characteristics of the devices. Specifically, we found that: i) a non-ideal, i.e. with Schottky-like behavior, p-contact influences the overall C-V characteristic of the device, especially at high forward voltages; ii) the C-V curves change in the presence of charge centers, which can affect the apparent charge profile (ACP) in different ways, depending on their physical location, by varying the amount of voltage required to sweep through the different layers of the active region; finally, we also showed that iii) the injection of electrons toward the active region, favored by the presence of tunneling through the first barrier, has detectable impact on the C-V characteristics. The approach proposed in this work ultimately provides a useful tool for the characterization of specific non-idealities present in electronic and optoelectronic devices, based on simple device-level C-V measurements.

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References

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[2] N. Roccato et al., APL, 122(16),161105 (2023)

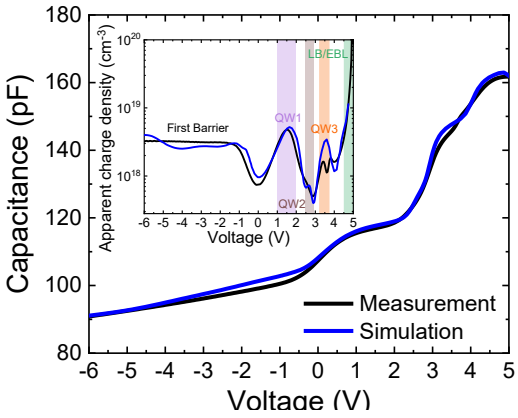

Figure 1 Measured vs. simulated CV profiles @ 1 MHz. The inset plot shows ACPs, from which specific device layers can be identified.