High Temperature Characterization of Deep Recessed N-Polar GaN HEMT

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GaN HEMTs are widely known for their use in RF applications due to their high electron mobility, saturation velocity, and breakdown field. GaN has a polar nature, where it can be grown in Ga-Polar or N-Polar orientation. However, it has been observed that N-Polar GaN HEMTs have superior performance than their Ga Polar counterpart as they can get better 2DEG confinement, ohmic contact, scalability, and pinch-off characteristics. To understand the limits of N-Polar HEMTs in sub-optimal environments, a series of measurements were taken at various temperatures above room temperature (25C). Through DCIV measurements at temperatures of up to 300C (573K), Ron and Ion/Ioff ratio were observed, showing the robustness of the HEMTs.

For this study an MOCVD grown deep recessed N-Polar GaN HEMT structure (Figure 1) with a 20nm of GaN Cap. The benefit of a GaN Cap is that it allows for better 2deg confinement, acts as passivation, and reduces DC-RF dispersion. The fabrication of these devices starts with initial alignment mark patterning and etching. After that hard mask of Si_3N_4, Al_2O_3, and SiO_2 is deposited, following with regrowth patterning and etching of hard mask and epitaxy until GaN channel is reached using wet and dry etching techniques. At this point highly doped n type GaN is grown via PAMBE and after growth, hard mask is removed using 1:1 mixture of HF: HNO_3. Then with a thin PECVD Si_3N_4 surface protection layer device isolation patterning and etch till buffer layer is done, following with insulating ion implantation with a thick photoresist as protection layer. After ion implantation, gates were pattern using optical lithography and the GaN Cap plus 2.6nm of AlGaN was etched using Atomic Layer Etching (ALE). Then after removing the thin Si_3N_4 protection layer, 7nm of MOCVD Si_3N_4 is deposited as dielectric. Finally, gate metal patterning and deposition is done, following with ohmic contact metal patterning, Si3N4 etching, and deposition. The final device structure is shown in figure 1.

For I_D-V_{DS} the goal of these measurements was to get r_{on} so we did not need to stress the devices far into saturation to see its peak current and to only see the keen, for that reason the measurements were taken from V_{DS} = 0V to V_{DS} = 2.5V at V_{GS}=0V at 25°C, 75°C, 150°C,225°C, and 300°C. Same for I_D-V_{GS}, a baseline of I_{on} /I_{off} = 1000 was chosen as to no stress the device and to achieve this gate bias, V_{GS}= -3.5V to 1V and drain bias, V_{DS} = 1V is set at 25°C, 75°C, 150°C,225°C, and 300°C. However, it is to be noted that these devices at 25°C can achieve I_{on} /I_{off} = 10^6. In figure 6, a trend is shown of I_{Dsat} decreasing as temperature is increased in equal increments of 75C, however the delta decrease from each 75C temperature step is reducing. As ΔI_{Dsat} from 225C to 300C is ΔI_{Dsat} = 0.068 A/mm, compared to 75C to 150C where ΔI_{Dsat} = 0.13 A/mm. Also, at 300C, r_{on} = 3.39 **Ω***mm, which is a 137% increase from 25C. The r_{on} vs Temperature in figure 4 of the devices with gate length(L_G) = 0.6 follows a similar increasing trend, but enlarging L_G to 1.5um, the r_{on} is increasing at a higher rate as temperature increases. Also, it is observed that I_{on}/I_{off} ratio is approximately constant as temperature increases as shown in figure 3, but at some points improves as temperature increases as seen with device with dimensions of L_{SD} = 2um and L_G = 0.6um.

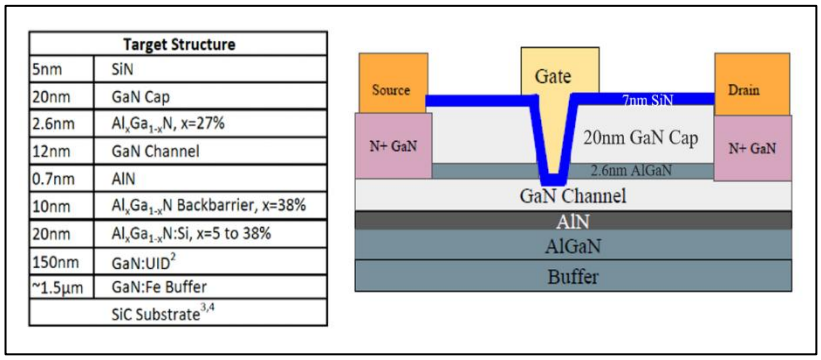

Figure 1: *MOCVD grown N-Polar GaN HEMT Epitaxy with 20nm of GaN Cap and Fully Fabricated Deep Recessed N-Polar GaN HEMT with MBE Regrown N+ GaN and 7nm of MOCVD SiN.*