Analysis of OFF-state Threshold Voltage Instability on Vertical GaN-on-Si Trench MOSFETs

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Introduction

GaN-based vertical devices on Silicon substrate are currently under study to provide a cost-effective alternative for Si- and SiC-based power devices targeting 1 kV and above. Despite the good performance of the devices, vertical devices are prone to several charge trapping processes involving deep levels in semiconductor and oxide layers [1], [2]. In this work, we will address the OFF-state induced threshold voltage instability in GaN trench MOSFETs.

Experimental Procedures

The devices under test consist of GaN trench MOSFETs (TMOS) grown by MOCVD on a Silicon substrate. The epitaxial structure consists of a strain-relief buffer layer, an n+-GaN drain layer, n^--GaN drift layer, a p^+-GaN body layer , and a n^+-GaN source layer. The gate oxide layer (SiO_2) was deposited by low-pressure chemical vapor deposition (LPCVD) at high temperature (880 °C) after the opening of the gate trench.

The threshold voltage instability of the devices was investigated by means of fast threshold voltage transients obtained with a custom experimental setup capable of applying arbitrary quiescent bias to the gate and drain terminals, that is periodically interrupted to perform an I_D-V_G measurement [1].

Results and Discussion

The experimental results, reported in **Figure 1(a)**, show that the devices present an increase of V_{TH} when the devices are stressed in OFF-state condition even for limited bias (10 V – 40 V) with a "saturating logarithmic" kinetic. The experiment performed for several combinations of $(V_G \leq 0\ V, V_D)$, shows that the negative gate voltage does not strongly affect the trapping mechanisms, thus suggesting the mechanism is due to the vertical epitaxial stack, rather than the gate module of the devices. The experiment repeated as function of temperature, revealed that the charge trapping process can be recovered only at high temperatures (> 200 °C) with an activation energy of approximately 1 eV. Capacitance deep level transient spectroscopy (C-DLTS) was performed on p-n diodes located on the same wafer, showing a good agreement of the main trap signature with respect to the one found during the V_{TH} transient experiments.

The interpretation of the model is reported in **Figure 1(b,c)**: when the device is in OFF-state conditions, the drain leakage promoted by the threading dislocations transports electrons from the source towards the p-body layer. Here, the electrons are trapped in deep level defects and result in an increase of the V_{TH} due to the negative charge [3].

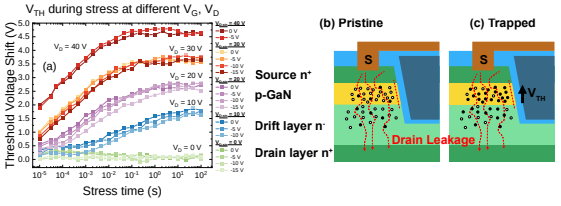

Figure 1: **(a)** Threshold voltage instability detected during OFF-state experiments with different gate voltages; **(b/c)** Charge trapping model.

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References

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