N-polar AlN-based transistors with enhancement-mode achieved using p-NiO_x gate stacks and suppression of sub-channel charge trapping in buffer layers

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Introduction

Enhancement-mode GaN-based high electron mobility transistors (HEMTs) for power electronics applications are now commercially available. However, charge trapping in sub-channel GaN buffer layers remains an issue affecting device stability and reliability [1]. N-polar AlN-based structures on sapphire substrates were recently demonstrated, featuring a thin surficial GaN channel layer and an associated 2-dimensional electron gas (2DEG) [2]. The ultrawide bandgap AlN back-barrier may suppress buffer trapping by enhancing 2DEG confinement.

Experimental Procedures

The device structure is shown in Fig. 1. The GaN channel thickness was 5 nm, and the AlN back barrier was 460 nm. Ti/Al/Ni/Au Ohmic contacts were alloyed at 500°C for 1 minute in nitrogen, providing low-resistance linear current-voltage (IV) characteristics. Plasma-enhanced chemical vapor deposition (PECVD) was used to form 20 nm SiN_x surface passivation layer, in which a window was opened using a low-damage plasma etch. P-type NiO_x (70 nm) was then sputter deposited via a lift-off process and annealed at temperatures between 250-450 °C. A Ni/Au gate metallization was then applied atop the p-type NiO_x. Gate length was 2.5 µm.

Results and Discussion

Transfer characteristics are shown in Fig. 1. For a p-type NiO_x anneal temperature of 250 °C, enhancement-mode operation is achieved, with a threshold voltage (V_{th}) of ~0.1 V. Increasing anneal temperatures results in more negative V_{th}, attributed to a reduced acceptor concentration in the NiO_x layer, confirmed using TCAD simulations and consistent with analogous III-polar enhancement-mode HEMTs that use p-type GaN gates [3]. When measured using drain bias pulsed-IV, the first-generation N-polar AlN-based transistors showed higher stability than commercial III-polar p-GaN gated HEMTs, confirming the effectiveness of the AlN back-barrier in suppressing buffer-related charge trapping.

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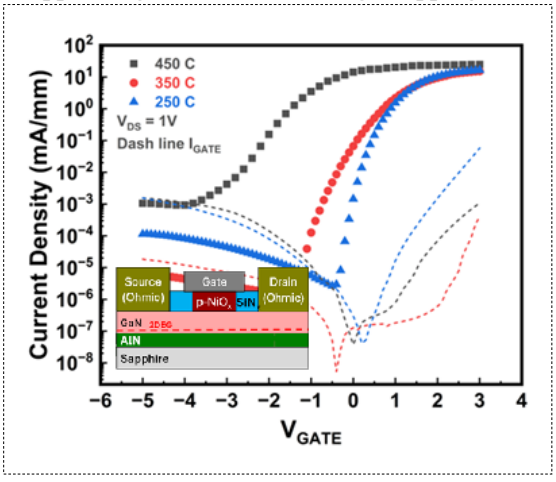

Figure 1 Effect of p-NiO_x anneal temperature on DC transfer characteristic. Inset: Device structure

References

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