Bias- and Temperature-Induced On-State Resistance Degradation in 650 V p-GaN HEMTs

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Introduction

Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) facilitate the development of power electronic systems with higher efficiency, faster switching, and reduced size [1]. To realise normally-off operation, essential for safe and practical circuit design, a p-GaN gate structure is typically introduced between the gate electrode and the AlGaN barrier. However, the stability of the p-GaN HEMT devices remains a major challenge, particularly under both positive and negative gate stress and elevated temperatures [2]. In this work, p-GaN gate HEMTs were subjected to controlled positive and negative gate bias stress across a wide temperature range in a thermal chamber. The study focuses on quantifying the variation of on-state resistance (R_{on}) under these conditions, and aims at providing deeper insight into the reliability and performance limits of p-GaN gate HEMTs in practical operating environments.

Experimental Procedures

The devices under test are Schottky p-GaN gate HEMTs (GPI65015DFN, 650 V/85 mΩ/15 A). A measurement-stress-measurement sequence was employed to evaluate the device performance. The devices were placed in a thermal chamber (TAS LTCL600) and tested over a temperature range of -50 °C to 150 °C in 25 °C increments. The gate-source voltages (V_{gs}) were 6 V and -10 V for positive and negative gate bias stress tests, respectively, within the operating range of the GaN HEMT devices. The variation of R_{on} was characterised using a source measuring unit (B2902A) after 1 ms, 10 ms, 100 ms, 1 sec, 10 sec, 50 sec, 100 sec, 500 sec, and 1000 sec of stressing time. During characterisation, V_{gs} was swept from 0-6 V, while the drain-source voltage (V_{ds}) was kept at 0.1 V.

Results and Discussion

The test results under different stress conditions are shown in Figure 1. Under positive gate bias, R_{on} decreased relative to the initial value, whereas negative gate bias led to a pronounced increase. At subzero temperatures, the drift in R_{on} was minimal. However, with increasing temperature, the rate and magnitude of variation became more significant. At the highest test condition of 150 °C, the reduction of R_{on} under positive gate bias may lead to increased power dissipation and potential thermal runaway due to positive feedback. In contrast, negative bias stress caused R_{on} to increase by 28.24%, which is detrimental to the efficiency of power electronic systems in application.

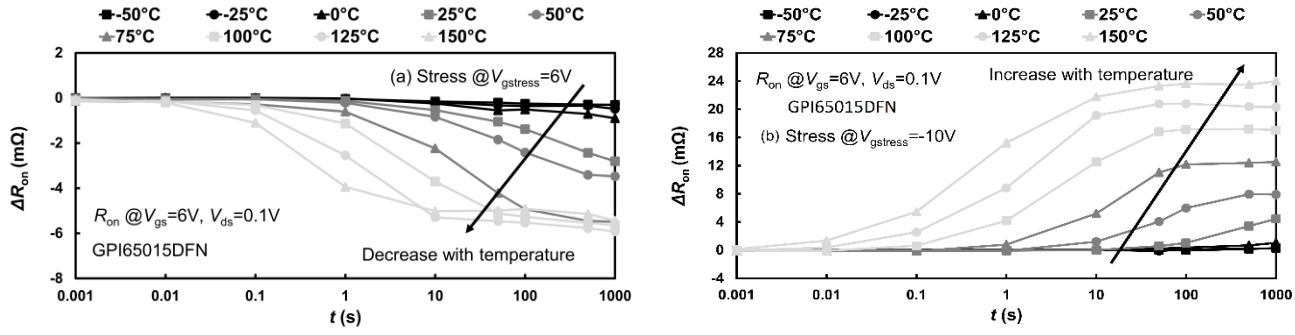

Figure 1. Drifts of R_{on} under positive and negative gate bias stress under different temperatures.

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References

[1] L. Gill, S. DasGupta, J. C. Neely, R. J. Kaplar and A. J. Michaels, IEEE Transactions on Power Electronics, 39 (1), 517-537,(2024)
[2] Z. Jiang, L. Li, C. Wang, J. Zhao and M. Hua, IEEE Transactions on Electron Devices, 69 (7), 3654-3659, (2022)