Study on the Improvement of Thermal and High-Frequency Characteristics of Multilayer Ceramic Capacitor Modules

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Introduction

DC link capacitors and resonant capacitors used in power converters occupy significant space within circuits, necessitating miniaturization and weight reduction. Consequently, efforts are underway to achieve miniaturization by replacing conventional film capacitors with modularized multilayer ceramic capacitors (MLCCs). Previous studies [1] have pointed out issues such as temperature variations in modules using multiple MLCCs, and new structures have been proposed. However, there has been little discussion regarding current imbalance and changes in frequency characteristics caused by the wiring structure of MLCC modules. Therefore, this study investigated these characteristics during the modularization process.

Experimental Procedures

Figure 1 shows the flat-structure MLCC module under analysis, consisting of 3 series and 5 parallel connections. MLCCs feature excellent frequency characteristics and high energy density, but their failure mode is short-circuiting. Therefore, they are used in multiple series connections to improve reliability. Furthermore, they are used in multiple parallel connections to ensure current capacity and capacitance. However, the following issues are considered:

- Heat dissipation characteristics vary with placement, potentially causing thermal concentration [1].
- Current imbalance is anticipated in each parallel path due to variations in parasitic inductance.

This study employs electromagnetic field simulation to clarify the latter issue and organize the challenges.

Results and Discussion

The analysis conditions involve applying a sinusoidal voltage with an amplitude of 5 V and a frequency range of 10 kHz to 40 MHz between terminals 1 and 2, as shown in Figure 1. The capacitance per MLCC is set to 500 nF, with the parasitic inductance of the MLCC denoted as L_{MLCC} and the wiring inductance as L_{wire}. L_{MLCC} was obtained from the MLCC datasheet, and L_{wire} was extracted using Ansys Q3D Extractor (manufactured by Ansys).

Figure 2 shows the current distribution characteristics for each parallel path. In this figure, the maximum and minimum currents flowing through each parallel path are normalized by their average values and displayed as error bars. This clearly shows that current variation is significantly more pronounced in the high-frequency band compared to the low-frequency band. This variation is caused by L_{wire} and leads to current imbalance during high-frequency operation. Therefore, when modularizing using multiple MLCCs, the wiring layout becomes a critical issue.

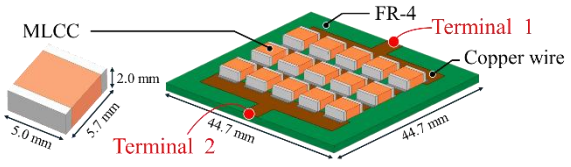

Figure 1 MLCC in 3 series and 5parallel

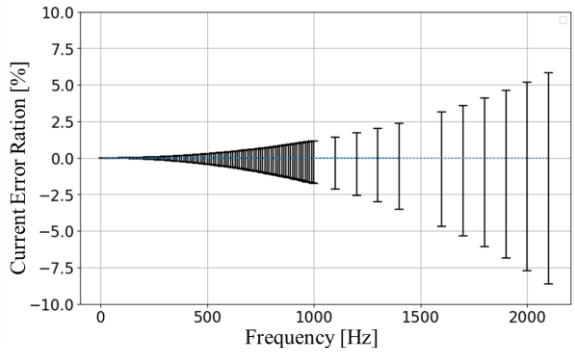

Figure 2 Analysis results of current distribution for each parallel path

Acknowledgement

This study investigated the impact of L_{wire} in MLCC modules. It was suggested that in the modularization of MLCCs, current imbalance and frequency characteristics can change depending on the wiring layout.

References

[1] S. Chowdhury et al,: IEEE Trans Transp Electrif, vol. 8, no. 2, pp. 2710-2720. (2022)