Novel surface passivation technique for GeSn alloy using GeO_2 atomic layer deposition

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Introduction

GeSn alloy semiconductor is a promising material for optical and electronic devices that can be monolithically integrated on Si ultra-large-scale integrated circuit platforms. We recently demonstrated room-temperature operation of resonant tunneling diodes (RTDs) based on GeSn/GeSiSn heterojunctions, with particular focus on crystal growth technology [1]. To further improve device performance, however, it is essential to establish a GeSn surface passivation technology that can effectively suppress surface leakage current. This requires both the reduction of interface state density (D_{it}) and control of the surface potential. In this study, we investigated the potential of GeO_2 as a passivation layer, owing to its well-known low D_{it} at the metal-oxide-semiconductor (MOS) interface [2]. We developed an atomic layer deposition (ALD) process using tetra-ethoxy germanium and ozone as precursors. Using this process, we demonstrated that ALD-grown GeO_2 is a promising candidate for surface passivation of GeSn-based devices.

Experimental Procedures

After chemical cleaning of n-type Ge(001) substrate (1.11–2.41 Ω·cm), ~200-nm-thick undoped $Ge_{0.948}Sn_{0.052}$ epitaxial layer and ~2-nm-thick Si-cap layer were grown at 150 °C using molecular beam epitaxy. The undoped GeSn epitaxial layer usually exhibits p-type conduction owing to the acceptor-like defect [3]. Then, mesa structures were fabricated by photolithography and reactive ion etching. Subsequently, a ~7-nm-thick GeO_2 layer and a ~50-nm-thick Al_2O_3 layer were deposited by ALD-method at 200 °C as the passivation layer. Following the formation of the passivation layer , the post O_2 annealing (POA) was performed at T_{POA}=300–400 °C for 30 min. Finally, contact holes were etched through the Al_2O_3/GeO_2 layers, and Al electrodes were deposited on both the top and bottom by vacuum evaporation. The current-density–voltage (J–V) characteristics of the fabricated p-GeSn/n-Ge diodes were measured.

Results and Discussion

Figure 1 shows the thickness of the GeO_2 layer on a Ge substrate as a function of the number of ALD cycles. The thickness increased linearly with the number of cycles, and a sufficiently high growth per cycle (GPC) of 0.35 Å/cycle was successfully achieved, which is consistent with previously reported values for GeO_2 ALD [4].

Figure 2 shows the J–V characteristics of p-GeSn/n-Ge diode. The introduction of an ALD-GeO_2 layer followed by POA was found to reduce the reverse current density. Detailed discussion of the results will be given during the presentation. Here, we evaluated the temperature dependence of J–V characteristics and the insulator/semiconductor interface properties based on the electrical characteristics of MOS capacitors. These results indicate that ALD-GeO_2 passivation combined with POA is generally effective for improving the performance of devices such as GeSn-based RTDs, as well as light-emitting and light-detecting applications.

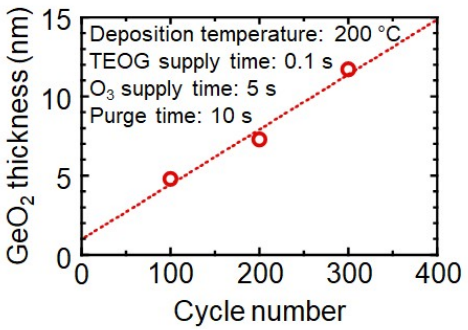

Figure 1 GeO_2 thickness as a function of ALD cycles, with the ALD process conditions presented in the graph.

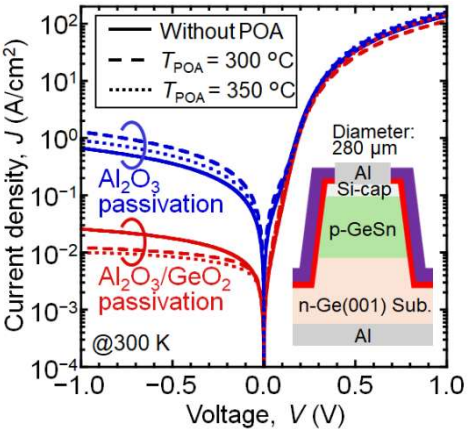

Figure 2 J–V characteristics of p-GeSn/n-Ge diodes passivated by Al_2O_3 and Al_2O_3/GeO_2. The electrode diameter is 280 μm.

Acknowledgement

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References

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