Evaluation of Insulator/GaN Interface Properties in MOSFETs with Floating Gate Structure

X. Li[1], M. Deki[2], H. Watanabe[3], S. Lu[3], J. Wang[3, 4], S. Nitta[3], Y. Honda[2-4], H. Amano[2-4]
[1]Department of Electronics, Nagoya University,
[2]D-Center, Nagoya University,
[3]IMaSS, Nagoya University,
[4]Institute for Advanced Research, Nagoya University
li.xigen.x4@s.mail.nagoya-u.ac.jp

Introduction

To realize the vertical GaN power MOSFETs, it is necessary to overcome the trade-off between achieving positive threshold voltage (V_{TH}) control and maintaining high channel electron mobility. Therefore, we applied a conventional Floating Gate (FG) structure, consisting of SiO_2/SiN/SiO_2 stack, to GaN-MOS devices. It is expected that positive shifts of V_{TH} and high channel mobility can be achieved simultaneously by electron injection into the FG layer. In this work, we evaluated the interface properties. In particular, the Flat-band voltage (V_{FB}) and Interface states density (D_{it}) of GaN-MOS capacitors with an FG structure were measured.

Experimental Procedures

Figure (a) shows the schematic of device structure. In Figure (a), The n-type GaN epitaxial layer was grown on the n^+-GaN substrate using MOVPE method. The effective donor concentration was calculated as 2.5×10^{16} cm^{-3} from *C-V* characteristics. FG structure (tunnel-SiO_2/SiN/block-SiO_2=5, 10, 12.5, 17.5, 20nm/5nm/35, 30, 27.5, 22.5, 20nm) was fabricated using sputtering and PECVD method. The gate electrodes and back contact were deposited by resistance heating method to avoid the generation of fixed charges and interface degradation during electrode formation process [1]. In addition, in order to improve the characteristics of the GaN/dielectric film interface, AlO_x interlayer was deposited by the Atomic Layer Deposition (ALD) method. After device fabrication, V_{FB} shift and interface characteristics were evaluated using *C-V* characteristics and conductance method [2].

Results and Discussion

Figure (b) shows the dependence of the measured ΔV_{FB} on the tunnel oxide thickness. In Figure (b), the V_{FB} approaches the ideal value as the t_{tunnel} increases. In addition, the linear dependence of ΔV_{FB} on the t_{tunnel} suggests the presence of fixed charges at the SiO_2/GaN interface. This fixed charge is considered to generate from plasma damage during the sputtering deposition of SiN, and such damage can be avoided when the t_{tunnel} is about 20 nm.

Figure (c) shows the D_{it} of the sample with a 20 nm tunnel oxide thickness, with and without the insertion of 5nm AlO_x layer. The sample without AlO_x exhibited a D_{it} on the order of 10^{12} $eV^{-1}cm^{-2}$, which is attributed to plasma damage during PECVD SiO_2 deposition. By inserting the AlO_x layer, the D_{it} was reduced by two orders of magnitude. This reduction suggests that the insertion of 5 nm AlO_x layer can effectively prevent plasma-induced damage on the GaN surface.

From these results, it can be concluded that FG-MOS capacitors with a low interface state density were achieved. In the presentation, the results of charge injection into the FG layer will be discussed.

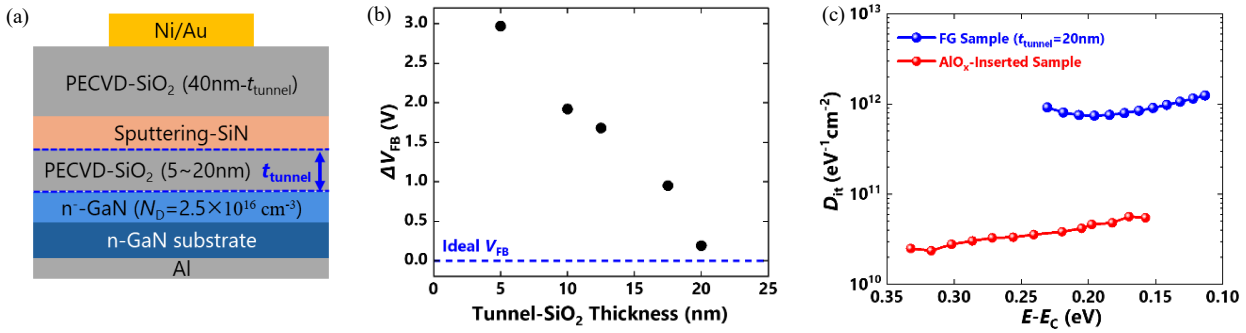

Figure: (a) The schematic of device structure. (b) The dependence of the ΔV_{FB} on the tunnel oxide thickness. (c) The D_{it} of samples w/wo AlO_x.

Acknowledgement

This work is based on results obtained from a project, JPNP24008, commissioned by the New Energy and Industrial Technology Development Organization (NEDO).

This work was also supported by Japan Science and Technology Agency (JST) as part of Adopting Sustainable Partnerships for Innovative Research Ecosystem (ASPIRE), Grant Number JPMJAP2311.

References

[1] Y. Ando et al., Appl. Phys. Express 17, 081001(2021).

[2] E. H. Nicollian, J. R. Brews, MOS Physics and Technology, Wiley-Interscience, 2002.