Evaluation of a surface conductive layer on etched u-GaN by C-V characteristics for charge balance evaluation of polarization superjunction GaN FETs

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Gallium nitride (GaN) polarization superjunction (PSJ) FETs are promising high-voltage power devices, achieving a breakdown voltage of over 1.2 kV despite their lateral layout.[1] In a superjunction, it is crucial to balance the charge amounts, as an imbalance leads to a decrease in breakdown voltage.[2] This study clarifies the effect of the surface state of the PSJ structure on its C−V characteristics.

The structure of the fabricated PSJ FET is shown in Fig. 1. The C−V characteristics were measured at a frequency of 100 kHz. The C−V characteristics exhibited a step-like change in gate-drain capacitance (C_{GD}). Fig. 2 shows the PSJ length (L_{PSJ}) dependence of C−V characteristics. Varying L_{PSJ} increased the capacitance in the small−$|V_G|$ region (V_G > -2 V, boundary at -2 V), whereas the plateau at -5 V ≤ V_G ≤ -2 V remained constant. This suggests that the former component originates from the PSJ region, where u-GaN is exposed by etching. The latter plateau is attributed to the unchanged p-GaN gate stack. It has been reported that the surface of etched GaN becomes n-type due to nitrogen vacancies.[3] Therefore, an n-type surface conductive layer may also be formed on the surface of the PSJ region, where p-GaN is removed by etching. TCAD simulations were performed under the assumption that a 5 nm-thick n-GaN layer was formed on the u-GaN surface via etching, as shown in Fig. 1. As shown in Fig. 3, the results indicate that the transition voltage in the small−$|V_G|$ region shifts according to the donor concentration of the assumed damaged layer. Fitting this transition voltage, the surface donor concentration was estimated to be approximately 3.4×10^{18} cm^{-3}. These results demonstrate that C−V measurement on PSJ structures is a non-destructive and simple method for evaluating the charge in the surface conductive layer introduced by etching.

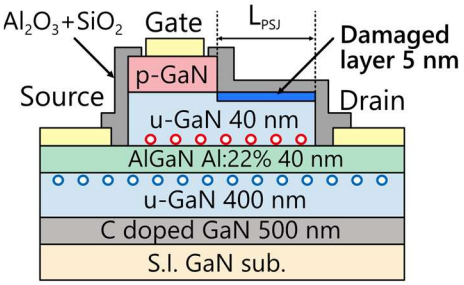

Fig. 1 Device structure of PSJ FET

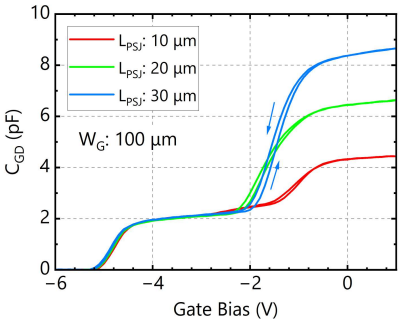

Fig. 2 C-V characteristics of PSJ FET

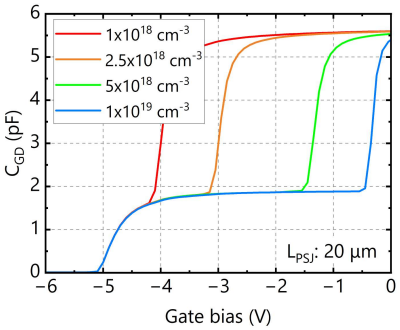

Fig. 3 Effect of N_D on C-V characteristics

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