Improvement of Electrical Performance of Te/TeO Thin Film Transistors Using Sputtering at Room Temperature

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ABSTRACT

Tellurium (Te) is promising material due to its excellent p-type semiconductor properties and power consumption efficiency. In this study, the electrical performances of the Te based transistors were demonstrated by adopting bilayer structure of Te / TeO

1. Introduction

Recently, with the rapid development of the electronic device industry, the necessity of developing an integrated circuit with capable of large-area manufacturing and low-temperature processing is increasing. However, the existing integrated circuit technology based on silicon has a problem of limitation in future flexible device applications due to their brittle nature. Therefore, need for technology that can replace the existing silicon-based technology and can manufacture a large area has increased, and organic semiconductors and oxide-based semiconductors are attracting attention as an answer to this.

In the case of organic-based semiconductors, the field effect mobility is at a very low level of 1 cm^2/Vs, and there is a fundamental instability problem due to the characteristics of organic materials. High electron mobility can be easily secured. However, most oxide-based semiconductors have poor hole mobility due to a local valence band. Therefore, better performance is required through the development of new semiconductors that can solve these problems.

For p-type AOS, it is difficult to achieve high electrical performance because the 2p orbital of oxygen constitutes the valence band (VB), and it is very difficult to localize holes by removing electrons from VB. In addition, since the effective mass of holes in VB is heavier than electrons in the conduction band (CB), it is difficult to manufacture a p-type semiconductor having excellent mobility. Although many candidates for high-performance p-type semiconductors have been presented so far, the easy and scalable realization of high-mobility p-channel TFTs has still been difficult.

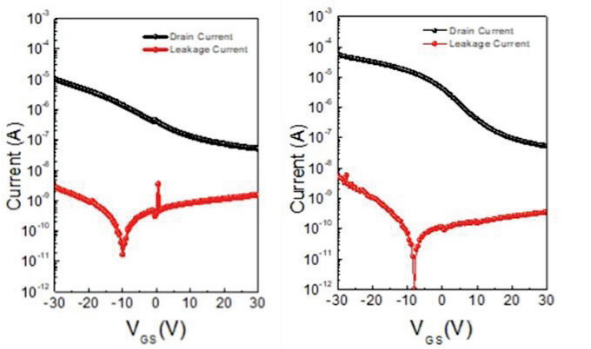
Here, a high-performance p-channel tellurium (Te)/tellurium oxide (TeO) TFT manufactured through a sputtering process at room temperature was fabricated. Te has become a new promising p-type material through the advantages of high mobility, narrow bandgap, high light absorption and good air stability, which offers great application potential in polarized infrared imaging, quantum information and photodetector applications. The fabricated Te/TeO TFT exhibits high field effect mobility and superior ION/OFF compared to Te TFT without complicated additional processes, and provides more stable properties. In addition, it was confirmed that the on/off ratio of the Te/TeO TFT (ALD-Al_2O_3) having a high dielectric constant was superior to that of the existing Te TFT. Finally, a small-sized Te/TeO TFT was fabricated through a photolithography process, and it was confirmed that all of them operate normally. Through this, the proposed Te/TeO device with uniform and stable performance is expected to provide new opportunities for expanding applications in integrated electronics and optoelectronic fields.

2. Experiment

p^{++} si wafer with an insulating layer of SiO_2(100nm) were used for the study. The substrates were cleaned in an ultra sonicator using acetone, methanol respectively. The target was subjected to pre-sputtering for 20min to reduce surface contamination. Te(10nm)/ TeO(30nm) deposition was performed at room temperature and fixed 10mTorr pressure during sputtering. The radio frequency (RF) power and Ar flow were fixed at 15W and 20 sccm. In the case of TeO, 0.3 sccm of oxygen was additionally added. After the deposition, the films were annealed in a RTA at 300 ^oC for 1 h in the ambient condition. and Au (100 nm) was deposited via thermal evaporation. The electrode deposition was performed at room temperature and ≈ 5 × 10^{-6} mTorr pressure. The active layer and the source-drain patterning process for manufacturing the transistor were performed using a shadow mask, and the width/length of the active layer was 800 μm and 200μm, respectively.

3. Result and Discussion

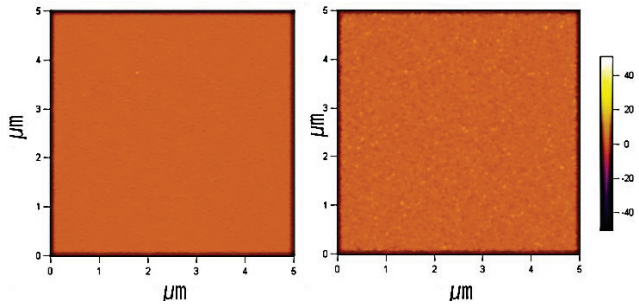
Fig 1 shows the transfer curves of Te and Te/TeO TFTs with the drain voltage of -1 V. By adopting Te/TeO bilayer structure, Te/TeO TFT shows the better electrical performance compare to single Te TFT.



Te **Te / TeO**

Fig 1. Improvement of Electrical Performance of Te / TeOThin Film Transistors High current than single Te

AFM surface morphological properties of Te and TeO films are shown in Fig 2 and the RMS values of Te and TeO films were 0.73nm and 1.07 nm, respectively. Since holes move through channels at the interface of the active layer/gate insulating layer, roughness is a factor that directly affects the electrical properties of the thin film transistor. Therefore, the Te/TeO thin film transistor with low surface roughness has excellent electrical properties.



Te: 0.73 nm **TeO:1.07 nm**

Figure 2. Comparison Surface Roughness Analysis of Te and TeO Films

The optical properties were measure in the wavelength range of 200–1000 nm. The transmittance of TeO and Te film were over 80 % and 20% at 660 nm, respectively.

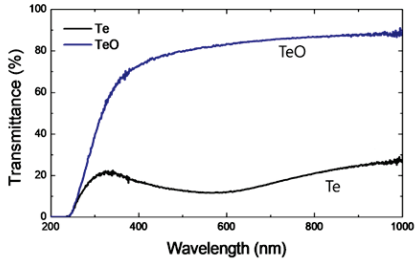


Fig 3. Comparison of Transmittance Analysis of Te and TeO Films

Figure 4 shows the output characteristics of the Te/TeO TFT, measured at -2 V intervals in a drain voltage sweep with a gate voltage step of 0 to -10 V, and shows no current crowding at all.

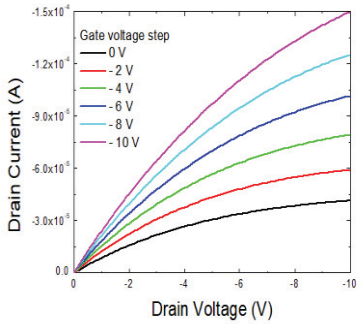


Fig 4. Output characteristics of Te/TeO transfer

Fig 5 shows the long term stability of Te / TeO TFT. Te / TeO TFT was stored in air room temperature ambient. The electrical performance does not changed after 1 week. This may due to the passivation effect of upper layer TeO.

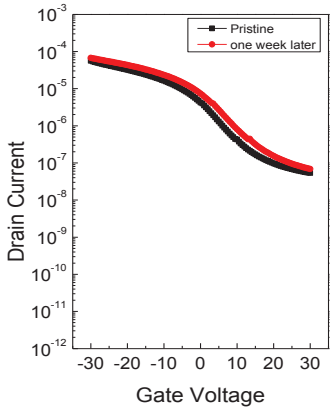


Fig 5. Threshold voltage (Vth) and field-effect mobility (μFE) are shown with the typical transfer curve (IDS-VGS) change of a Te/TeO TFT after one week.

4. Conclusions

In this study, the effect on the electrical properties of Te/TeO thin films and thin film transistors based there on through sputtering deposition at room temperature was investigated. Room temperature fabricated Te/TeO TFT has good electrical performance with a mobility of 20 cm^2/Vs, I_{on}/I_{off} ratio of 10^5

We show that sputtered Te thin films are attractive materials for p-FETs processed at room temperature and that when they have a Te/TeO bilayer structure, monolithic 3D circuits with higher performance compared to single Te as well as flexible, transparent and large-area electronics We were able to confirm that it has an

important practical meaning in the device. We believe that further improvements in thin film quality will enhance the device performance of Te or Te/TeO FETs. Integrating a p-FET using Te with an n-type FET such as a-IGZO can not only compose a 3D CMOS circuit, but also use the existing silicon CMOS circuit to further expand/improve the system performance for line back-process electronics and It has the advantage of being able to implement it.

5. Reference

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