# Quantum Technology Using Modern Materials Engineering to Create Better Qubits with Lower Error Rates

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**ABSTRACT**

*Quantum technology promises to be a new paradigm for important fields including computation, communication and metrology. Materials engineering of quantum devices is critical to achieve high fidelity performance. This paper describes how integrated cluster tools can enable high quality interfaces for superconducting quantum devices.*

## 1 Introduction

Quantum computing offers the potential to radically improve the computation power used to solve some of the most difficult and important problems that we face. In contrast to classical computers, quantum computers require quantum bits (or qubits) as the building blocks for information. Qubits are coherent two-level systems of quantum mechanical systems that need to be controlled and manipulated to realize computation.

By harnessing quantum mechanical resources, such as the superposition state of a qubit and entanglement of qubits, quantum computers can exploit new algorithms to solve difficult computational problems [1]. There are several critical requirements to build a quantum computer [2]. The ability to precisely control the state of the qubits to realize low error gate operations are crucial to realize the computation power required to demonstrate valuable applications.

Many different physical implementations have been realized ranging from superconducting qubits, photonic quantum computing, spin qubits, trapped ions, neutral atoms and color centers. Each hardware type offers different advantages and challenges in terms of realizing low error rates and scaling to large numbers of qubits.

Quantum computing hardware has seen significant progress over the past decade. Systems have grown from a handful of qubits to more than hundreds. Additionally, two qubit gate error rates have decreased from the few percent level to the 0.1% level in many different systems. However, to make a useful quantum computer, the number of qubits and the qubit errors rates need to be improved further (Fig. 1).

At the same time, over the past decade there have been considerable advancements in the semiconductor device fabrication industry to make the current and future nodes. Materials engineering of surfaces and interfaces at the atomic scale have enabled breakthroughs for gate-all-around transistor technology and back-end-of-line (BEOL) wiring. Additionally, advanced packaging and 3D integration have emerged as critical technologies to enable high-bandwidth compute power for applications like artificial intelligence.

Quantum computing technology can benefit from the latest developments in the semiconductor industry. Materials engineering of surfaces and interfaces can be critical to reduce losses or errors of qubits. Advanced packaging of quantum processing components is needed to build large and powerful quantum computers with high yield. Further, photonic interconnects can be used to connect quantum computing modules to further increase the size of the system.

Amongst the different quantum computing technologies, superconducting qubits are one of the leading platforms [3]. Superconducting qubits operate at microwave frequencies (10 MHz to 20 GHz) and are composed of superconducting metal films patterned on a low loss dielectric substrate and Josephson junctions, which are composed of a thin insulator between two superconducting materials. The main advantages of superconducting qubits include fast gate operations (~10-100 ns) and state-of-the-art gate fidelity (two qubit gate error rates ~0.1%). Additionally, the qubit parameters can easily be tuned by changing the circuit parameters and enabling novel qubit designs to reduce sensitivity to various noise sources. Lastly, superconducting qubits can be manufactured using similar methods to make semiconductor devices [4], which will be critical for scaling.

## 2 Methods and Discussion

One critical challenge of superconducting qubits is further decreasing the error rates by increasing the coherence times of the qubits. Coherence times are typically limited by dielectric or two-level system (TLS) losses of surfaces and interfaces of the superconducting materials. These interfaces are typically denoted as the substrate-metal (SM), substrate-air (SA) and metal-air (MA) interfaces. The losses of a superconducting qubit or resonator can be characterized by $\frac{1}{Q_l} = \sum_i p_i \tan\delta_i$, where $Q_l$ is the quality factor and $p_i$ and $\tan\delta_i$ are the participation ratio and the loss tangent in the volume $i$, respectively [5]. State-of-the-art superconducting qubit

quality factors are near $Q_l$~$10^7$. Although ~90% of the electric field energy resides in the bulk of the substrate, the loss tangent of amorphous surfaces and interfaces are typically ~$10^3$-$10^4$ larger compared to the bulk of low loss substrates and are the dominate loss factor.

There are two main mechanisms to minimize the losses from the surfaces and interfaces. The first is to decrease the participation ratio. This can be done by modifying the design of the superconducting circuit or by reducing the thickness of the surface layer using improved fabrication methods. The second method is to decrease the loss tangent of the surface by reducing the disorder of the materials at the interface.

One of the critical interfaces is between the substrate and the superconducting metal layer (SM interface). Due to the high permittivity of the substrate relative to the air above, the participation ratio of the SM interface is relatively large and one of the dominating loss factors.

The impact of the SM interface thickness and loss tangent was simulated in COMSOL. A coplanar waveguide (width, *w*, = 10 μm, gap, *g*, = 6 μm and metal thickness, *t*, = 100 nm) operating at *f* = 5 GHz and made from superconducting aluminum was studied (Fig. 2a). The substrate material was silicon ($\epsilon_r$ = 11.7). We assumed the SM interface had a relative dielectric constant of $\epsilon_r$ = 3.9. We modified the thickness and loss tangent of the SM interface to see the effect on the quality factor (Fig. 2b). We focus on the losses of the SM interface and neglect other loss sources for this simulation.

By decreasing the thickness of the SM interface from 5 nm to 0.5 nm, the quality factor increased by ~8x. Additionally, the quality factor linearly increases with a decrease in the loss tangent. This highlights the importance of optimizing the SM interface during the fabrication of superconducting qubits.

We used a 300 mm integrated vacuum cluster platform to engineer the SM interface (Fig. 3a). The cluster platform enabled multiple chambers to be optimized for individual processes (i.e. surface preparation or material deposition) and wafers are transported between chambers in vacuum using a robotic arm. This enables complex materials engineering solutions without breaking vacuum and maintaining high quality interfaces.

We demonstrate the ability to have sharp interfaces between a silicon substrate and a superconducting aluminum film. We started with a 300 mm silicon wafer as the substrate. First, the silicon surface was cleaned in a vacuum chamber to remove the native oxide with minimal surface damage. This enables deposition of aluminum on a clean silicon surface without breaking vacuum and prevents oxidation of the clean silicon surface. The 100 nm aluminum film was deposited using physical vapor deposition (PVD) onto the clean silicon surface.

We used a scanning transmission electron microscope (STEM) to characterize the silicon and aluminum interface after the deposition and observe a sharp, sub-nm thick interface between silicon and aluminum (Fig. 3b). Oxygen and other process related elemental impurities were not observed within electron energy loss spectroscopy (EELS) detection limit at or near the SM interface. By significantly reducing the thickness of the silicon and aluminum interface, the losses at the silicon and aluminum interface can be greatly reduced.

## 3 Conclusions

Superconducting qubits are a promising platform to realize a quantum computer. One of the main challenges is improving the materials engineering of the superconductor interface and surfaces to decrease the losses of the circuits. In simulations, we showed that decreasing the thickness and loss tangent of the SM interface can play a significant role in increasing the quality factor of the circuit. Lastly, we demonstrated that an integrated cluster tool can provide a materials engineering solution to enable sharp interfaces between a superconducting aluminum film and the silicon substrate.

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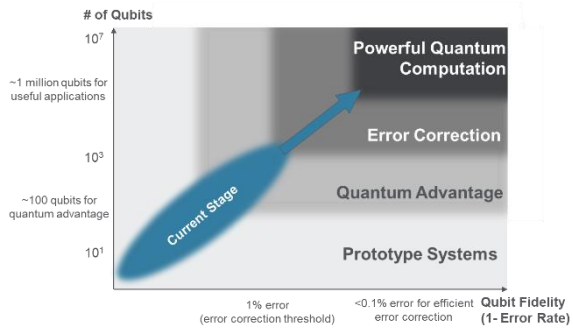


**Fig. 1 Roadmap for quantum computing.**

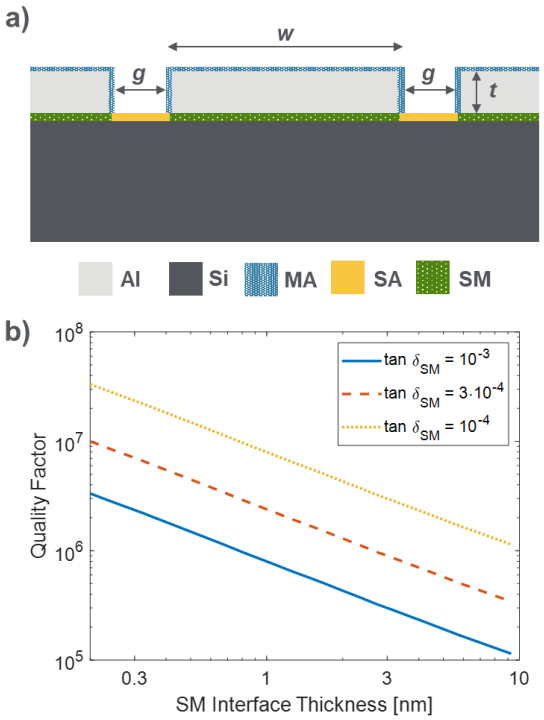


**Fig. 2 a) Coplanar waveguide geometry indicating the different surfaces and interfaces. b) Simulation result of a coplanar waveguide quality factor as a function of the SM thickness and loss tangent.**

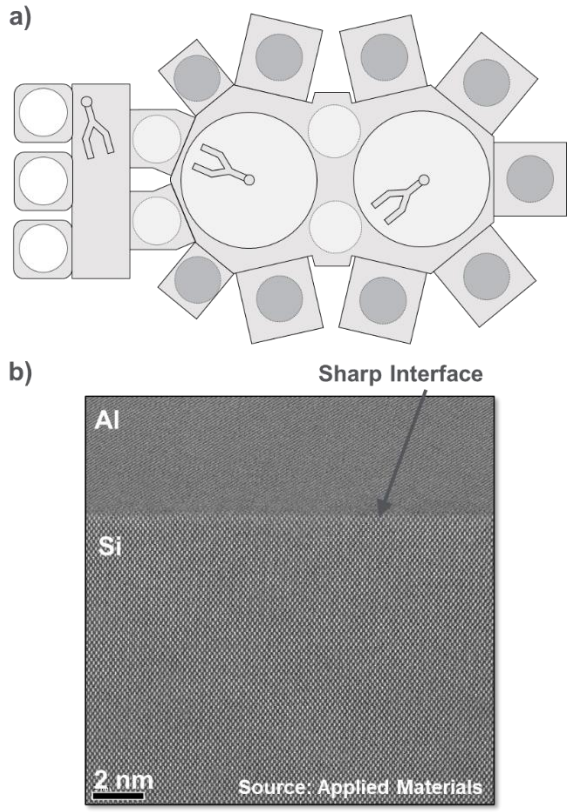


**Fig. 3 a) Schematic of an integrated vacuum cluster tool platform used to fabricate superconducting materials. b) STEM image of the sharp aluminum silicon interface.**