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Developing high-performance p-type oxide TFTs and CMOS circuits

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ABSTRACT

The integration of high-performance p-type oxide thin-film transistors (TFTs) is crucial for achieving fully complementary metal-oxide-semiconductor (CMOS) circuits in next-generation flexible and scalable electronics. However, the limited electrical performance and instability of p-type oxide semiconductors have hindered their widespread application. In my talk, I will discuss our recent progress in developing p-type oxide-based TFTs, with a particular focus on our latest advances in amorphous tellurium oxide (Te-TeO$_x$) materials. Furthermore, we integrate these high-performance p-type TFTs with n-type oxide TFTs to realize flexible large-scale CMOS circuits with balanced electrical characteristics and low power consumption.

1 Introduction

The rapid advancement of flexible and transparent electronics has driven the demand for high-performance complementary metal-oxide-semiconductor (CMOS) circuits (Figure 1) [1]. While n-type oxide thin-film transistors (TFTs) have demonstrated exceptional electrical properties and stability, the development of p-type oxide TFTs remains a significant challenge due to their inherently low hole mobility, high defect densities, and limited operational stability. Overcoming these limitations is critical for achieving fully complementary logic circuits with low power consumption and high integration density [2].

In this presentation, we discuss the development of high-performance p-type oxide TFTs from the conventional copper oxide semiconductors via a low-cost solution process, which exhibit enhanced hole transport characteristics and improved stability [3,4]. By optimizing the channel composition, we achieve amorphous tellurium suboxide with high hole mobility, high current ratio, and excellent bias stress stability, addressing key bottlenecks in p-type oxide electronics [5]. Furthermore, we demonstrate the successful integration of these optimized p-type oxide TFTs with well-established n-type oxide TFTs to construct flexible, large-scale CMOS circuits. The resulting circuits exhibit balanced electrical characteristics, improved energy efficiency, and mechanical flexibility, making them highly promising for applications in wearable electronics, transparent displays, and next-generation computing systems.

2 Results and Discussions

In my talk, I will mainly present a new approach to designing amorphous p-type semiconductors based on a mixed phase of high-mobility tellurium embedded within an amorphous tellurium suboxide matrix (Te-TeO$_x$, $0 < x \leq 2$). Amorphous Te-TeO$_x$ thin films were deposited via thermal evaporation of TeO_2 powder, followed by low-temperature annealing at 225 °C in ambient conditions. Selenium (Se) alloying was achieved by blending Se with TeO_2 prior to evaporation, maintaining the amorphous nature as confirmed by X-ray diffraction (XRD) and high-resolution transmission electron microscopy (HRTEM), as shown in Figure 2.

To evaluate the electronic properties, bottom-gate, top-contact TFTs were fabricated using Ni source/drain electrodes on a 100 nm SiO_2 dielectric. Pristine Te-TeO$_x$ TFTs exhibited p-channel behavior with a hole mobility (μ_h) of 4.2 $cm^2/V{\cdot}s$ and an on/off current ratio (I_{on}/I_{off}) of ~10^4. Se alloying significantly improved performance, with optimized devices (Se/Te = 1/3) achieving μ_h of ~15 $cm^2/V{\cdot}s$, I_{on}/I_{off} of ~10^7, and stable onset voltages (~20-25 V). Excessive Se incorporation, however, led to performance degradation due to n-type doping effects. Electrical characterization, including output curves and transmission-line method analysis, indicated Ohmic contacts with a low contact resistance of ~200 Ω·cm (Figure 3).

Bias stress tests demonstrated excellent operational stability, with minimal threshold voltage shifts (~3.2-3.4 V over 5400 s) and negligible defect generation. Unlike conventional p-type oxides (Cu^+, Sn^{2+}) and emerging halide-based semiconductors, Se-alloyed Te-TeO$_x$ exhibits superior ambient stability, addressing key reliability concerns. The scalability and processability of Se-alloyed Te-TeO$_x$ were validated through photolithography-compatible patterning and high uniformity across 4-inch wafers. The wafer-scale deposition process is cost-effective (~USD 0.3 per film) and high-throughput (seconds per layer), making it suitable for industrial adoption.

We integrated Se-alloyed Te-TeO$_x$ TFTs with n-type

oxide TFTs to realize complementary logic circuits (inverters, NAND, NOR gates, ring oscillators, and large-scale flexible CMOS ICs). The CMOS inverters exhibited full-swing operation, rapid voltage transitions, and a high voltage gain, with an 82% noise margin. NAND/NOR gates demonstrated ideal rail-to-rail outputs, confirming the potential of fully complementary oxide-based logic circuits. This work paves the way for high-performance, scalable, and cost-effective p-type oxide semiconductors, accelerating the development of flexible, low-power CMOS electronics.

Building on recent progress in amorphous p-type Te-TeO_x semiconductors, which demonstrated controllable hole transport through self-formed Te networks within an oxide matrix, we further explore redox-assisted approaches for low-temperature modulation of carrier concentration and network connectivity. Here, we introduce a sulfur-mediated redox strategy that enables in situ formation of Te conduction channels and effective hole doping under a low thermal budget (~120 °C) [6]. This approach pro-vides a practical route to enhance transport properties and integration compatibility, addressing the long-standing challenge of achieving stable, high-performance p-type oxide thin-film transistors at low temperatures.

The introduction of sulfur effectively modulates the local bonding environment by promoting TeO_2 dissociation and partial reduction of Te^{4+}, which facilitates in situ formation of interconnected Te nanophase channels. The resulting S-TeO_x films exhibit a hole mobility of ~12 $cm^2/V{\cdot}s$ and an on/off ratio exceeding 10^6, both more than an order of magnitude higher than undoped counterparts processed under identical conditions. The devices also show excellent reproducibility, stability in air, and compatibility with flexible substrates.

By integrating the sulfur-engineered p-type Te-TeO_x TFTs with n-type InGaZnO transistors, we realized a range of all-oxide CMOS circuits on both rigid and flexible substrates. The inverters exhibit a voltage gain as high as 1694 with clear rail-to-rail output, while five-stage ring oscillators reach oscillation frequencies up to 339 kHz at V_{DD} = 12 V. Beyond basic logic units, large-scale CMOS circuits were also demonstrated with high functional yield and operational stability (Figure 4), highlighting the scalability of this approach. These results establish sulfur-mediated redox engineering as an effective route to advance amorphous p-type oxides from material development to circuit-level integration, offering a viable pathway toward low-temperature, large-area, and flexible electronic systems.

3 Conclusions

We propose Te-TeO_x as a promising amorphous p-type candidate for next-generation flexible and low-power CMOS electronics, paving the way for highly scalable, energy-efficient, and industrially viable p-type oxide semiconductors. Future work will focus on further device miniaturization, power efficiency optimization, and expanding circuit complexity to enhance real-world applications.

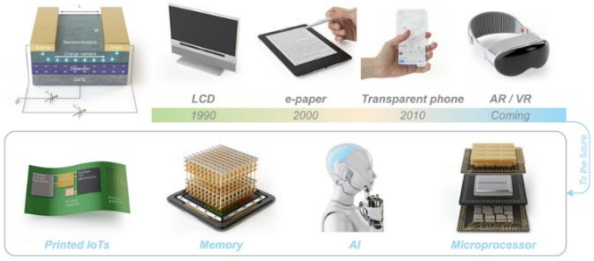

Fig. 1. Schematic TFT architecture and the revolution of TFT technology in displays and the future application prospects.

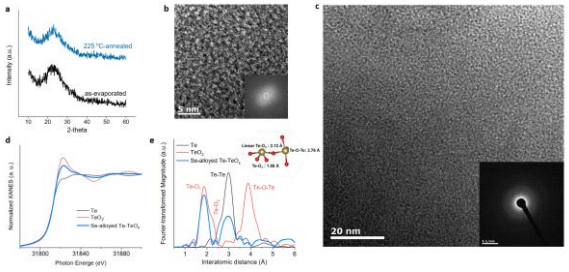

Fig. 2. a, XRD spectra of as-evaporated and 225 °C-annealed Se-alloyed Te-TeO_x thin films on glass. b,c, HRTEM images, the fast Fourier transform spot patterns, and selected area electron diffraction pattern of 225 °C-annealed Se-alloyed Te-TeO_x. d, Te K-edge XANES spectra of the Se-alloyed Te-TeO_x film and reference materials of elemental Te and TeO_2. e, Corresponding FT of Te K-edge k^3-weighted EXAFS spectra. The inset shows the tetragonal TeO_2 bonding model.

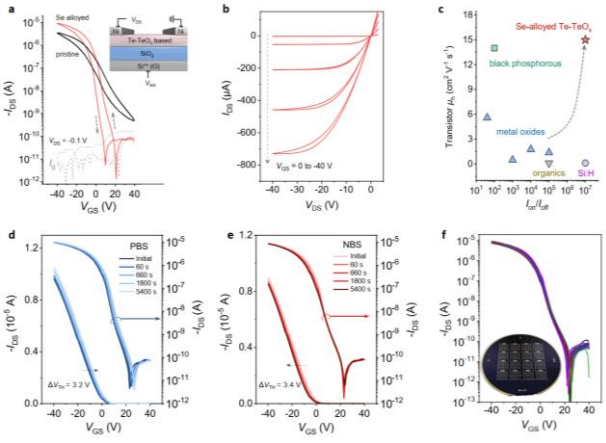

Fig. 3. a, Transfer characteristics of pristine Te-TeO_x and Se-alloyed Te-TeO_x TFTs; the inset shows TFT geometry (both hysteresis direction is counterclockwise). b, Output curves of one Se-

alloyed Te-TeO_x TFT. c, Benchmark of μ_h and I_{on}/I_{off} of reported amorphous p-channel TFTs. d,e, Transfer curves and the V_{TH} shifts of Se-alloyed Te-TeO_x TFTs under PBS and NBS tests with different time durations. f, Transfer curves of 80 randomly measured TFTs fabricated via optimised condition. The inset shows the optical image of TFT arrays on a 4-inch SiO_2 wafer.

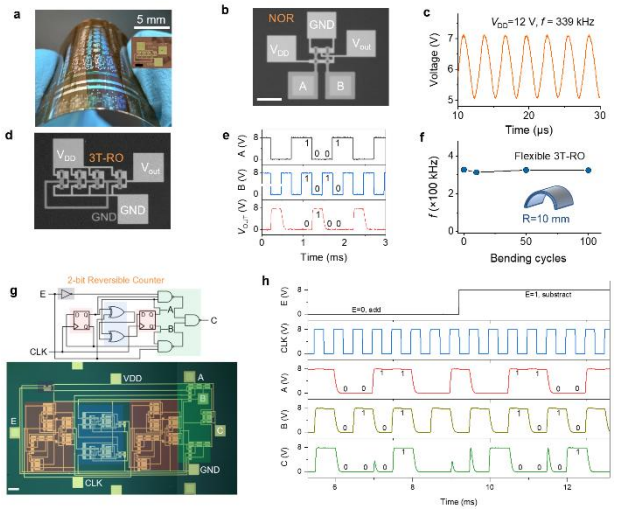

Fig. 4. a,b,d, Image and output waveform of the CMOS NOR gate based on the p-type TeO_x:S and n-type IGZO TFTs. c,d Oscillation frequency at different bending times of the flexible 3-stage RO on PI. e, Output waveform of the CMOS NOR gate based on the p-type TeO_x:S and n-type IGZO TFTs. g,h, Optical image and dynamic input-output waveforms of the 2-bit reversible counter.

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