Advanced High-mobility Multilayer TFTs Using Dynamic PVD Gas Separation System

**Yujiro Takeda[1], Wei-Chun Ma[1], You-Ron Lin[1], Elliot Lu[1],
Dejiu Fan[2], Jung Bae Kim[2], Lynn Yang[1], Juergen Grillmayer[1], Zero Hung[2],
Marcus Bender[3], Soo Young Choi[2]**

yujiro_takeda@amat.com
[1]Applied Materials, Tainan Display Lab, Tainan, Taiwan
[2]Applied Materials, Inc., Santa Clara, USA
[3]Applied Materials GmbH & Co. KG, Alzenau, Germany
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ABSTRACT

We investigated high-mobility multilayer TFTs using the dynamic PVD system. The gas separation unit allows comparable TFT performance without a significant increase footprint. The resulting TFTs demonstrate a high field-effect mobility of 26.2 $cm^2/V\cdot s$. In addition, process optimizations enabled the reduction of the channel length to 2 μm, and improved PBTS reliability, with ΔV_{th} 0.8 V.

1 Introduction

Metal oxide semiconductors (MOx) thin-film transistors (TFTs) have expanded their applications in display backplanes due to their relatively high mobility, low off-leakage current, and adaptability in manufacturing display panel factory [1]. Key TFT specification for future displays includes maintaining low off-leakage characteristics while achieving higher mobility, enhanced reliability, and short channel performance. In recent years, development of TFTs using high-mobility oxides (HMO) has been particularly active [2-4]. The objectives of this development are to improve the specifications required for displays, reduce the area of peripheral circuits, and lower costs. It is known that TFT characteristics become narrower with increased mobility. In order to address these challenges, previous studies have suggested that stacking different types of channel materials is effective [5-9]. We have studied that capping layers either at bottom or on top can be used to improve TFT properties, Including initial characteristics and reliability. We first examined device configurations that would facilitate stacking from the perspective of film coating in physical vapor deposition (PVD) [10]. We evaluated single films using microwave photoconductivity response (μ-PCR) and confirmed TFT characteristics [11]. Furthermore, we optimized the process condition for high-mobility multilayer. We evaluated the created TFTs using a semiconductor analyzer and evaluated their reliability. Finally, we report on the direction for improving initial characteristics and reliability using HMO and In-Ga-Zn-O (IGZO) multi-stacked layers.

2 Experiment

For TFT fabrication, 150nm thick molybdenum (Mo) is coated as the bottom-gate (BG). Then, 100 nm of SiNx and 300 nm of SiOx are continuously deposited as BGI by PECVD. The metal oxide was deposited with the New Aristo, using magnetron sputtering for Gen.6. In this experimental work, IGZTO was used for HMO. After patterning and annealing, gate insulator (GI) layer is deposited with thickness of 150nm by PECVD. A Ti/Mo (30nm/250nm) metal was deposited by sputtering and patterned as the top gate (TG). The GI layer is patterned by plasma dry etching, and plasma treated to form n^+ region. Interlayer dielectrics (ILD) of SiOx/SiNx (400nm/ 100nm) was coated using PECVD and via holes are patterned. Finally, 30nm/250nm thick Ti/Mo layer is coated and patterned for source and drain electrodes. All the device properties are measured by Keysight B1500A. The TG voltage is applied from -20V to +20V while BG was connected to the source electrode. the potential applied to the TG during PBTS (V_g= +30V, 70°C) and NBTIS (V_g= -30V, 70°C, 2000 nits) for 1 hour.

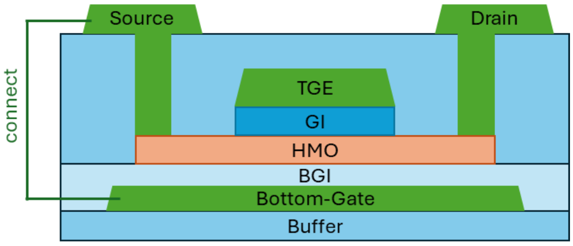


Fig.1 Schematic image of cross-sectional HMO top-gate TFT device structure.

3 Results

3.1 PVD Gas separation

Typically, a multilayer with HMO and IGZO structure requires different gas environments for each metal oxide layer. The layers need to be either coated separately, that is, in two chambers that are separated by lock valves

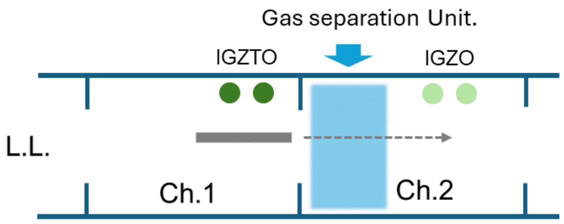
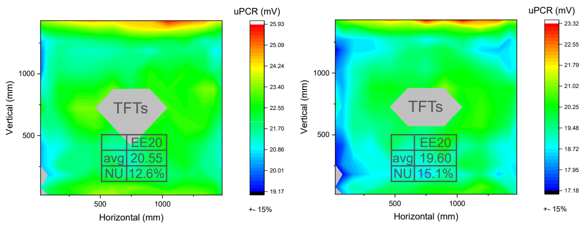


Fig.2 The concept image of the gas separation hardware configuration in the dynamic PVD system.



(a) Actual gas separation (b) Perfect gas separation

Fig.3 μ-PCR maps of as-deposited HMO/IGZO dual layer stack on glass with comparison of (a) "Actual gas separation" and (b) "Perfect gas separation".

(as in a static PVD system) or by very long distance in a dynamic PVD system to ensure gas mixing is limited. Gas diffusion during the HMO materials coating process in dynamic PVD systems can significantly hinder the performance and reliability of TFTs. Traditional methods to mitigate this often involve depositing individual layers in separate vacuum chambers, leading to increased processing time and complexity. To address this challenge, an advanced hardware design has been integrated into the New Aristo dynamic PVD system. This innovation enables multilayer PVD coating within a dynamic TWIN PVD system, offering significant tool footprint or mass production capacity improvement over existing approaches. Design detail of the gas separation module will not be disclosed due to IP protection.

As shown in Fig. 2, HMO and IGZO is deposited in Ch.1 and Ch.2 chambers, respectively. From internal study, the best coating conditions for HMO and IGZO are both at 0.5Pa but 80% O2 and 40% O2, respectively. The need for different O2 concentration during process allows us to evaluate the performance of the gas separation (GS). We have the "actual GS" case, and the "perfect GS" case to make the comparison.

For the "actual GS" case, Ch.1 chamber is filled with 0.5 Pa, 80% O2, while Ch.2 chamber with 0.5 Pa, 40% O2. The deposition of HMO and IGZO is done continuously, without having the substrate returning to load lock (L.L.). For the "perfect GS" case, both HMO and IGZO layers are deposited while the entire PVD system is filled with the designed gas conditions, i.e., 0.5 Pa 80% O_2 and 0.5 Pa 40% O_2, respectively. First, the bottom HMO layer is coated in 0.5 Pa 80% O_2 atmosphere, and the substrate returns to L.L. After that, the gas condition of the whole PVD system is changed to 0.5 Pa 40% O2, and then the IGZO top layer is deposited. In this way, we can guarantee that no gas crosstalk is possible, hence, a simulated "perfect GS".

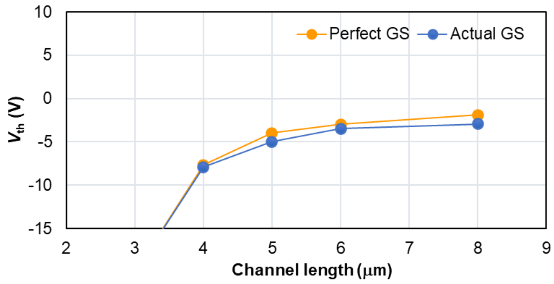


Fig. 4 The V_{th} position change along channel length from 8 μm down to 3 μm with channel width = 4 μm.

Fig. 3 shows that both cases produce as-deposited film with comparable μ-PCR sum amplitude. The gray areas in the μ-PCR maps in Fig. 3 are the positions on the mother substrates where the TFT wafers are attached. Fig. 4 exhibits the threshold voltage (V_{th}) position change along channel length from 8 μm down to 3 μm with channel width=4 μm. One can see that the V_{th} tendency of the two cases is comparable, that is, the two cases show same process window. Further optimization is possible to shift overall V_{th} position more positive and allow larger process window. This approach enables continuous multilayer deposition under multiple process gas conditions without increasing the tool footprint or giving up the dynamic deposition nature (best film uniformity, high throughput) within the dynamic PVD system.

3.2 Process optimization

As mentioned in the previous section, the device performance can be optimized from the status as in Fig. 4. In the following sections, we will go through stack modeling, short channel performance, and reliability, each working on an improvement direction, aiming to reach an optimized device integration for future application.

3.2.1 Stack modeling

The stack modeling in multilayer structure is a critical choice. As high mobility is pursued, the channel layer thickness must be kept thin to prevent V_{th} from becoming negative. We fixed the top layer thickness at 50 nm and the bottom layer thickness at 150 nm and compared the TFT characteristics when HMO was placed at the top and bottom. Fig. 5 shows the I-V characteristics and reliability PBTS results of fabricated dual-active-layers TFTs. The results indicate that the TFT with HMO at the bottom exhibited a mobility of 24.2 cm²/Vs. The V_{th} was

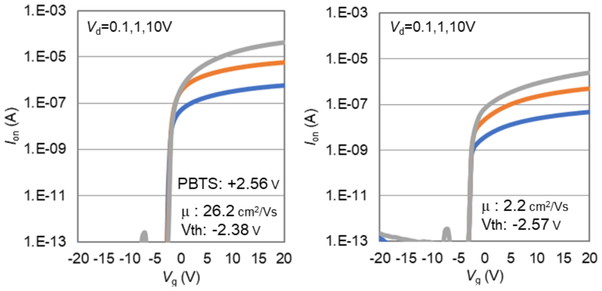


Fig. 5 Initial I-V characteristics of HMO/IGZO and IGZO/HMO multilayer TFT.

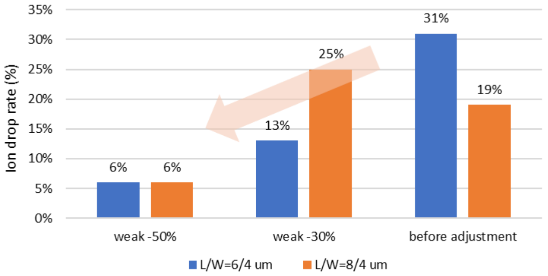


Fig. 6 Dry etching adjustment result with IGZO/HMO multilayer TFTs to reduce I_{on} drop rate (%).

-2.3 V, and the PBTS exceeded 2 V, indicating room for improvement. On the other hand, compared to the IGZO-top structure, V_{th} negative and significant low mobility were observed in TFTs with HMO at the top. Regarding V_{th} minus, the structure with IGZO as the upper layer is expected to act as a hydrogen blocking layer. Although V_{th} remained almost the same, the decrease in Ion suggests that the root cause lies in the process rather than the material. We considered that HMO was damaged and etched out during dry etching. To address this issue, the dry etching conditions were adjusted. Fig. 6 shows the Ion drop occurrence rate when the dry etching conditions were changed from strong to weak. As a result, it was confirmed that the weak dry etching conditions reduced the frequency of I_{on} drops.

On the other hand, since the failure rate of I_{on} drop did not become zero even after adjustment, we identified that placing HMO at the top narrows the process margin. Therefore, we decided to fix the structure to HMO/IGZO and proceed with further process improvement. Nevertheless, further process optimization will lead to improvements in the IGZO/HMO structure.

3.2.2 Short channel performance

In this part, we focused on improving short channel performance. There are various methods for improving short channel performance, one of the most effective approaches is the application of doping. We performed B^+ doping to n^+ the top IGZO layer. Additionally, we adjusted the ILD and GI conditions to an oxygen-rich to prevent TFT depletion. Typically, in the GI cut structure, where GI and ILD adjustments can be made independently, adjustments become easier. However, it becomes relatively difficult to adjust GI and ILD while remaining GI on n^+. The plot of V_{th} versus L length for devices under these conditions is shown in Fig. 7. The results clearly show an improvement in short-channel performance. It suggested that short channel performance can be improved by optimizing the final carrier density within the channel and the ΔL region at the channel end. In a structure with IGZO placed in the top layer, IGZO plays the role of blocking hydrogen, as mentioned above. Therefore, the improvement effect of the upper layer is effective. Fig. 7 shows that the PBTS of the TFTs under the improved short channel performance conditions is nearly the same, indicating no improvement. Therefore, the following section will focus on discussing improvements to PBTS.

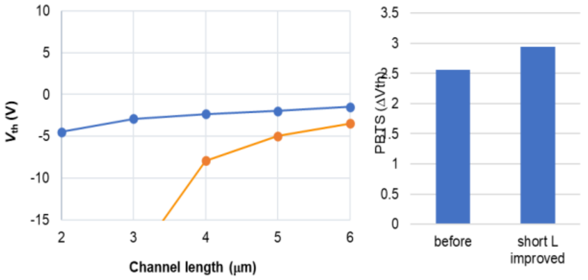


Fig. 7 Initial I-V characteristics and PBTS ΔV_{th} of HMO /IGZO multilayer TFT before and improved short L.

3.2.3 PBTS reliability improvement

When focusing on PBTS, attention is typically given to the channel-GI interface trap. The most effective and simple method for improving GI film quality is to increase the deposition temperature. Fig. 8 shows the initial characteristics and PBTS results of TFTs with high-quality GI applied for reliability improvement. GI was deposited with high temperature from 320°C to 340°C on the multilayer channel. The mobility and V_{th} of TFTs maintain almost the same values, but PBTS show a considerable improvement from 2.56 V to 0.8 V.

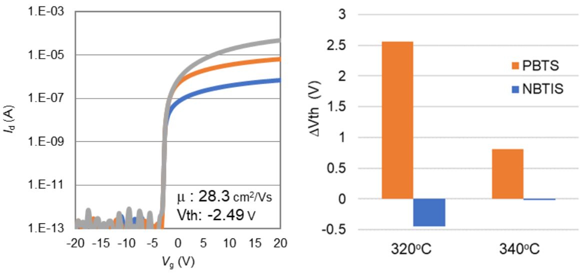


Fig. 8 Initial I-V characteristics and PBTS ΔV_{th} of HMO /IGZO multilayer with high quality GI.

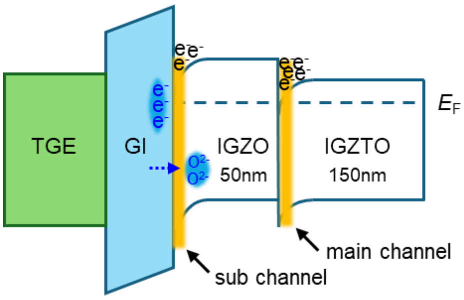


Fig. 9 The schematic energy band diagram of the PBTS mechanism with top gate HMO/IGZO multilayer TFTs.

This result gives us some special indications. Because this TFT has a multilayer and the HMO material is located on the bottom side, there is no interface contact with GI. Generally, the band diagram of a multilayer semiconductor with different mobilities is as shown in Fig. 9 [7-8]. The high mobility side becomes the main channel and the IGZO side becomes the subchannel based on the number of electrons swept by V_g.

Based on the above considerations, the following reasons for the improvement in PBTS can be assumed. First, the electronic trap in GI interface was reduced by improving the GI film quality. Second, excess oxygen diffused from the GI for trapping electron and creates a deep sub gap in IGZO, was reduced in high quality GI film. As a result, the electrons trapped at the GI or IGZO/GI interface decreased, and the positive shift in V_{th} is suppressed.

From the results described above paragraph, the HMO multilayer structure gives us another degree of freedom to improve TFT characteristics, and the gas separation function enables multi-active-layer deposition without increasing tool footprint and impacting throughput. By further pursuing this structure, we expect to be able to achieve higher mobility in oxide TFTs and realize panel specifications equivalent to those of LTPS.

4 Conclusion

This work demonstrates that the New Aristo dynamic PVD system with gas separation enables stable multilayer IGZO TFT fabrication under multiple gas conditions. μ-PCR mapping and device results confirm consistent film and short-channel performance in terms of threshold voltage. We also investigated the potential of multilayer channel structures. The HMO/IGZO multilayer improves process margin and achieves a mobility of 26.2 cm²/V·s. The short-channel performance was optimized by the B^+ doping and quality of the GI and ILD, achieving TFT operation even at a 2 μm channel length. In addition, increasing the GI deposition temperature improved PBTS stability, reducing ΔV_{th} from 2.56 V to 0.8 V.

These findings highlight the process flexibility of multilayer structures and their suitability for next-generation display applications.

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