Dual-Metal Source Contacts Double the Programming Speed in LTPS Pixel Circuits with Contact-Controlled TFT Switches

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ABSTRACT

Source energy barriers enable contact-controlled transistors to achieve excellent performance as pixel drivers due to early saturation and flat output curves. Their low off-state leakage is attractive for switch applications; however, low on-current may limit transient performance. Introducing a dual-work-function contact significantly improves transient behavior for a range of barrier heights.

1 Introduction

Low temperature polycrystalline Si (LTPS) remains a favored technology for many display applications, despite its many challenges, e.g. kink effect and off-state leakage. Considerable efforts in thin-film transistor (TFT) architecture design (Fig. 1a) and circuit techniques [1]–[6] have improved performance over the years, but off-currents are still too high, which lead to power waste and flicker, especially in low refresh rate applications. Low temperature polysilicon oxide (LTPO) [7] has certainly advanced the state-of-the-art, however this further complicates manufacturing, as well as increases associated costs, water use, emissions, etc.

Contact-controlled transistors, such as the multimodal transistor (MMT, Fig. 1b) [8], do not suffer the same shortcomings as conventional Ohmic-contact TFTs. As MMT's adopt charge injection principles from source-gated transistors (SGTs) [9]–[12], they share many benefits, including early saturation, flat output characteristics, improved uniformity, robustness to electrical stress [13], and low off-currents [14]. However, these features are largely traded-off for lower drain currents, which has limited SGT use to low-power applications, such as drive transistors in display pixel circuits [11], [15].

Recently, we have demonstrated that the source energy barrier, a necessary requirement for contact-controlled operation, can be designed to be low enough for MMTs to be used for both switch and drive transistors in pixel circuits [16], [17]. However, optimization of barrier height can be complex, given that a contact metal with precisely the required work function is not always available. Here, we demonstrate that using a dual-work function (DWF) source contact [18] allows not only for higher switch currents but also for flat saturated drive currents at low supply rail voltage. A simple one-transistor 1-capacitor (1T1C) demonstrator circuit was simulated using Silvaco Atlas to conform the performance of MMTs with DWF source (DWFMMTs, Fig. 1c,d)) over regular MMTs (Fig. 1b).

2 Experiment

LTPS TFTs with Ohmic contacts (Fig. 1a) and MMTs (Fig. 1b), and DWFMMTs (Fig. 1c,d), were simulated in Silvaco Atlas with default, previously verified, LTPS materials and models [2], [14]. See Table I for device and materials parameters. For off-state leakage behavior, Shockley Read Hall, band-to-band and phonon assisted tunneling models were used, as validated in [2]. Selberherr's impact ionization was enabled for hot-carrier effects [8]. $2.3 \cdot 10^{19}$ cm^{-3} *n*-type doping under source and drain was included for the TFT, as well as 1 µm *n*-type gate-overlap low drain doping (LDD) of

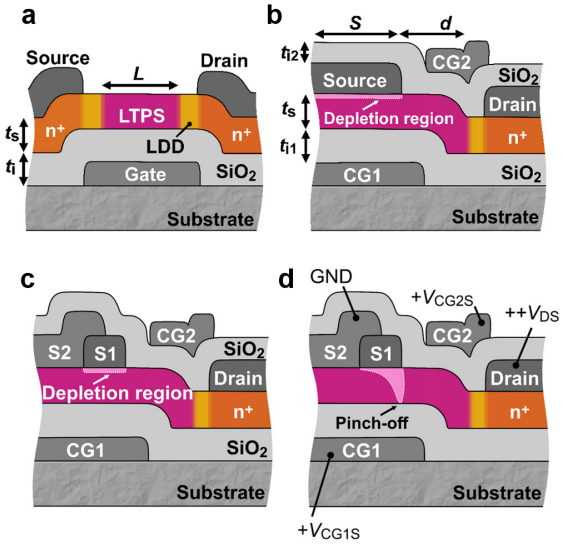

Fig. 1. Cross-sections of a) LTPS TFT with low drain doped (LDD) contacts; b) MMT with current control gate (CG1) and switching gate (CG2); c) DWFMMT with Schottky metal source (S1) and Ohmic source (S2). d) Full depletion under the S1 due to the reverse biased energy barrier.

$4.6 \cdot 10^{17}$ cm^{-3} to reduce off-state carrier generation, as per [2]. No field relief structures were implemented. MMT and DWFMMT architectures included doping only at the drain to make its contact Ohmic, with the same values as used in the TFT for comparison, and the work function (*WF*) of the source contact (or the source metal S1 of Fig. 1c of DWFMMT) was varied. Metal S2 of the DWFMMT was set to 4.17 eV to model an Ohmic contact. No contact doping was included under the source. Source metal S1 resides next to the source-drain gap, *d* (Fig. 1c).

Silvaco's Mixed-Mode capability was used to simulate 1T1C circuits, with TFT, MMT, or DWFMMT as the switch, C1 = 0.3 pF, and transistor width *W* = 3 µm.

Table I: Device simulation parameters

Parameter	MMT, DWFMMT (S1)	TFT
Contact work function, *WF* [eV] (S2 *WF* = 4.17 eV)	4.17, 4.37, 4.42, 4.47, 4.52, 4.57, 4.62	4.17
SiO_2 relative permittivity, ε_i	3.9	
Gate insulator thickness [nm], t_{i1}, t_{i2}, t_i	100, 60	60
LTPS thickness [nm], t_s	30	
LTPS electron, hole mobility [$cm^2V^{-1}s^{-1}$]	300, 30	
Source-CG1 overlap [µm], *S*	2, 1 (S1)	–
Source-drain Separation [µm], *L* or *d*	3	

3 Results and Discussion

3.1 Device Characteristics

Transfer characteristics for an Ohmic-contact TFT, MMT, and DWFMMT are shown in Fig. 2a, with the off-state of both MMT and DWFMMT being over an order of magnitude lower than that of the TFT, due to the source (or S1) energy barrier [14]. Naturally, the on-state drain current is lower, due to contact-controlled operation. For the same *WF* of the source or S1 metal of the DWF device, on-current is significantly higher, due to the recently described Mode III charge injection [18]. Mode I injection refers to thermionic-field emission at the source edge [9], whereas in Mode II injection a proportion of saturation voltage V_{DSAT1} is dropped in the network of resistances in the semiconductor along S1 [10], [19]. The remainder of V_{DSAT1} that reaches the Ohmic S2 interface will be dropped at the edge of S2, which leads to a large amount of current, which requires higher V_{DS} to pinch-off at the source edge (at V_{DSAT2} [19]). Lower values of S1 *WF* lead to higher injection (Fig. 2b) but inevitably result in loss of contact-control if the energy barrier is too low to fully pinch-off the accumulation layer at the edge of the source [19]. Also shown in Fig. 2b (which are the transfer characteristics for the current control gate, CG1), is the ability for CG1 to turn the device off even if the channel control gate (CG2) is biased such that the channel region is fully accumulated [8]. This is a hallmark of MMT operation.

MMT behavior is further demonstrated in the transfer characteristics for CG2 (Fig. 2c), whereby for low CG1-source voltage V_{CG1S}, the transistors with moderate-to-high *WF* require lower CG2 voltage to sufficiently accumulate the channel and ensure its resistance does not interfere with modulation of injection (i.e. the curves flatten) [8]. For higher V_{CG1S}, only the highest barrier allows the device to operate as an MMT at higher biases. This behavior, however, can be useful for exploiting the device to be operated as a switch in the on-state, with the advantage of the energy barrier preventing unwanted off-state leakage.

Even though the drain current of contact controlled transistors can saturate at low drain-source voltage [11], when operated as switches in emissive pixel circuits, such devices are not required to operate in saturation. The voltage that will be programmed onto the storage capacitor corresponds to the value of the DATA signal [16], [17]. To attain the required on-current for driving the OLED, this value will be in the 1-3 V, which falls mostly in the linear/triode region of the output characteristic of the DWF switch transistor, where the DWFMMT and TFT have similar current capabilities. Fig 2d shows that unlike

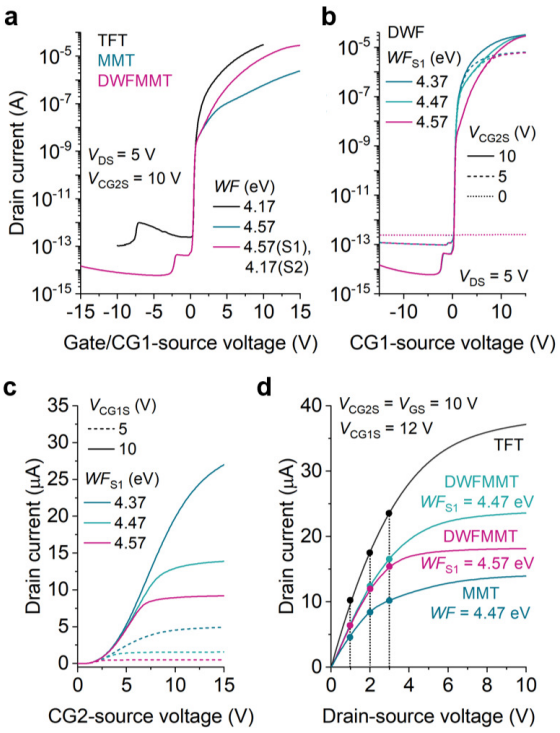

Fig. 2. a) Transfer characteristics for TFT, MMT, and DWFMMT. b) CG1 transfer characteristics for DWFMMT showing the device can turn fully off even if channel highly accumulated. c) CG2 transfer characteristics for DWFMMT showing independence of drain current on CG2 bias at low voltage or high work function *WF*. d) Output curve comparison for MMT, DWFMMT, and TFT.

the conventional MMT, the DWFMMT can maintain a drain current which is much closer in magnitude to that of the TFT even for a S1 energy barrier which is higher than that used for the MMT. Accounting for the potentially higher overall gate capacitance of contact-controlled transistors, in the first order, charging the storage capacitor with a TFT or with a DWFMMT switch should take similar amounts of time.

3.2 1T1C Circuit Demonstration

The 1T1C circuit (Fig. 3a) is intended to replicate the operation of the switch transistor [16], [17]. During the programming phase of pixel operation, the switch (T1 or M1) is required to rapidly charge, and equally importantly, discharge a storage capacitor C1 to the DATA potential when the select signal SEL is asserted on its gate. M1's gates have been connected together, for simplicity, however there are benefits to driving them at different potentials at the expense of increased signaling complexity, such as for mitigating or indeed promoting hot-carrier effects [20], or for performing advanced circuit operation in a compact footprint [21], [22]. The voltage stored on C1 is the voltage that appears on the gate of the drive transistor (denoted as output voltage VOUT).

The performance of charging/discharging T1 is as expected from a device with symmetrical contacts, unlike M1 which has an energy barrier at the source. The decision to connect either source or drain to DATA would depend on the application. For limiting off-state leakage, the source should be connected to DATA. During emission, assuming that the DATA node is grounded, the rectifying contact will be at a lower potential than the Ohmic one [17]. While a regular MMT as M1 is capable of charging and discharging the capacitor in the required time frame (Fig. 3b), it can only perform as well as a conventional TFT for a limited range of *WF* (Fig. 3c, top). The limits of this range depend on the interplay with the channel, therefore carrier mobility will play a role. This imposes limits on what metals can be used to create the required energy barrier. Indeed, Schottky contacts are the simplest to realize, but if barrier tuning with additional processing steps is required, it might be more convenient to implement the DWF approach. The DWFMMT as M1 can charge/discharge the capacitor practically as fast as the TFT for a wider range of *WF* and with reduced effects of parasitic coupling. Thus, even where high Schottky barriers are used for the S1 portion of the MMT's source (Fig. 1), there is little penalty to on-current magnitude.

4 Conclusions

Contact-controlled transistors, such as source-gated transistors and multimodal transistors, have widely been excluded as switches in display pixel circuits, due to concerns that energy barriers would limit the on-current. Yet, because of their superior off-state operation, such devices deserve reconsideration. We have previously shown how source barrier height can be tailored to deliver

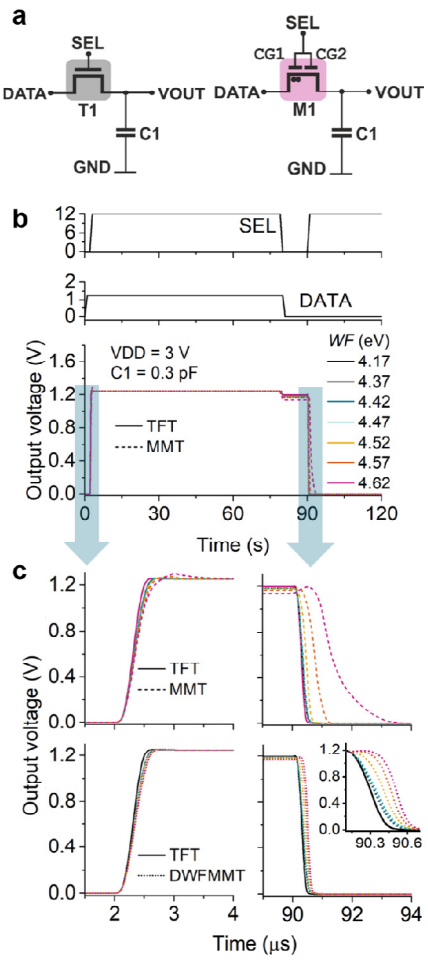

Fig. 3. a) Circuit schematics with the dual-metal contact of the DWFMMT indicated by two dots, and b) circuit timing diagrams. c) Detail of the rising and falling transients of the VOUT potential vs. MMT (top) and DWFMMT (bottom) source/S1 contact *WF*. Inset for zoom in of fall time.

sufficient drain current. The new approach presented here uses the dual-metal source contact which can deliver significantly higher on-current than the conventional Schottky contact for double the charging speed of the storage capacitor, while retaining the necessary off-state performance for leakage reduction.

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