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Tin halide perovskites for high-performance thin-film transistors and circuits

Huihui Zhu*

*hhzhu@uestc.edu.cn
School of Physics, University of Electronic Science and Technology of China, Chengdu, China.
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ABSTRACT

In this talk, I will present our breakthrough in developing high-performance p-channel perovskite TFTs through composition engineering using both solution processing and thermal evaporation approaches. By employing triple-cation compositions in solution processing and lead chloride ($PbCl_2$) modification in thermal evaporation, we demonstrate high-performance TFTs and their successful implementation in complementary logic circuits.

1 Introduction

The rapid advancement of flexible and transparent electronics has driven the demand for high-performance complementary metal-oxide-semiconductor (CMOS) circuits[1]. While n-type oxide thin-film transistors (TFTs) have demonstrated exceptional electrical properties and stability, the development of p-type oxide TFTs remains a significant challenge due to their inherently low hole mobility, high defect densities, and limited operational stability. Overcoming these limitations is critical for achieving fully complementary logic circuits with low power consumption and high integration density.

The recent development of tin (Sn^{2+})-halide perovskites, such as caesium tin triiodide ($CsSnI_3$), methylammonium tin triiodide ($MASnI_3$), and formamidinium tin triiodide ($FASnI_3$) have marked a pivotal shift in high-performance p-channel thin film transistors (TFTs). These materials are known for their intrinsic p-type semiconducting properties, characterized by exceptionally low effective mass, low Fröhlich interaction, weak ion migration, and intrinsically high hole mobilities, ranging over hundreds of square centimeters per voltage second[2]. To apply these high-mobility perovskites as channel layers for TFT applications, it is crucial to modulate the excessive hole concentration and control the crystallization process to extend the scattering time ($\mu = q\tau/m^*$). Recent efforts have reported composition engineering methods to regulate the nucleation and crystallization of solution-processed Sn^{2+}-halide perovskite precursors, enabling TFTs to achieve high hole field-effect mobilities (μ_{FE}) over 50 $cm^2\ V^{-1}\ s^{-1}$, rivaling those of low-temperature poly-silicon (LTPS) devices[3, 4]. The significance of Sn^{2+}-halide perovskites represents the rise of an emerging p-type semiconductor, showing potential for practical application in next-generation complementary electronics integrated with commercial n-channel metal-oxide technology.

In this presentation, I will discuss the development of high-performance p-type Sn^{2+}-halide perovskites TFTs, processing from initial 2D layered structures to 3D multiple compositions, while exploring both solution process and thermal evaporation approaches. By structural and crystallization control, we realize high-performance Sn^{2+}-halide perovskites TFTs with μ_{FE} over 70 $cm^2\ V^{-1}\ s^{-1}$, on/off ratio over 10^8, surpassing LTPS benchmarks[2, 3]. Specifically, we demonstrate thermal evaporated p-channel Sn^{2+}-halide perovskite $CsSnI_3$ TFTs using $PbCl_2$ as a reaction initiator to trigger solid-state conversion, enabling high-performance and industrially compatible devices[5]. Furthermore, we integrate the obtained p- with n-type metal oxide transistors to create complementary inverters with high gain and logic gates showing rail-to-rail switching. In the meantime, we observe negligible ion migration effects in these Sn^{2+}-halide perovskites TFTs[6, 7].

2 Results and Discussions

In my talk, I will mainly present vapour-deposited high-performance and stable inorganic $CsSnI_3$-based p-channel TFTs with the key additive of $PbCl_2$. The unique volatile chloride can initiate solid-state reactions and extend for complete perovskite phase formation, promoting densely packed enlarged grains in cascaded manner. The optimized TFTs exhibit μ_{FE} over 40 $cm^2\ V^{-1}\ s^{-1}$ and on/off current ratios (I_{on}/I_{off}) over 10^8, along with long-term stability. We also demonstrate the large-scale uniform fabrication of Sn^{2+}-halide perovskite TFT arrays, overcoming the technical challenges previously identified in the solution-process. The unique characteristics of vapour-deposition in thin film crystallization herald a significant step forward in the application of Sn^{2+}-halide perovskite materials in electronics through an industry-compatible method.

To deposit the $CsSnI_3$-based perovskite channel layer, a sequential deposition method was used for each component—$PbCl_2$, SnI_2, and CsI—to avoid contamination and ensure precise control of the atomic ratio (Fig.1a). $PbCl_2$ was deposited as the initial layer on the 100 nm SiO_2 dielectric substrate, followed by the sequential evaporation of SnI_2 and CsI layers. The deposition of $PbCl_2$ in the bottom layer plays a key role in

achieving high-quality film deposition, which will be discussed later.

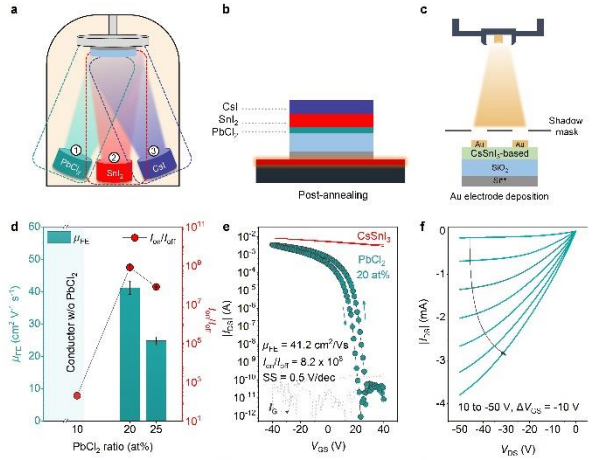

Fig. 1. a,b,c Fabrication of bottom-gate, top-contact vapour-deposited $CsSnI_3$-based TFT (a) sequential evaporation of perovskite compounds, (b) post-annealing treatment of the perovskite multi-layers, (c) evaporation of Au electrodes. d, Field-effect mobility and on/off current ratio as a function of $PbCl_2$ molar ratio. Error bars represent the standard deviation of sample size n = 10. e, Transfer characteristics of $CsSnI_3$ TFTs and optimized $CsSnI_3$:$PbCl_2$ TFTs ($Cs_{1.3}SnPb_{0.2}I_3Cl_{0.15}$). I_G indicates gate leakage current. Channel length/width = 100 μm/200 μm (V_{DS} = -40 V). f, Output characteristics of optimized $CsSnI_3$:$PbCl_2$ TFTs.

The multi-layer films were then annealed at 320 °C to merge and form a single $CsSnI_3$ layer (Fig.1b). The sample with $PbCl_2$ will be further referred to as the $CsSnI_3$:$PbCl_2$ film. The final step involved the deposition of Au source/drain electrodes to construct bottom-gate, top-contact TFTs (Fig.1c). For the pristine $CsSnI_3$ TFT, a metallic behaviour with poor field-effect modulation is observed (Fig.1d,e). This phenomenon indicates a high hole concentration (n) in the $CsSnI_3$ channel, measured to be ~10^{18} cm^{-3} using Hall measurements. The corresponding output characteristics of the optimized $CsSnI_3$:$PbCl_2$ TFT exhibit good linearity at low drain-source voltage (V_{DS}) and current saturation at high V_{DS}, indicating a low charge-carrier injection barrier and ohmic contact between the channel layer and electrodes (Fig.1f).

We then performed film characterisations from the surface to bulk to understand the mechanism behind the formation of $CsSnI_3$ in vapour-deposition and the unique roles of $PbCl_2$. The scanning electron microscopy (SEM) images of $CsSnI_3$:PbX_2 films illustrate a distinctive difference from pristine $CsSnI_3$ to PbX_2-incorporated films (Fig.2a). To characterise and trace the Cl incorporation in the $CsSnI_3$-based thin film, we conducted X-ray photoelectron spectroscopy (XPS) analysis and depth profiling. The deposited $CsSnI_3$ films exhibit evenly distributed elements of Cs, Sn and I throughout the bulk, indicating successful reaction amongst precursor compounds (Fig.2b). In addition, a uniform distribution of Pb was detected throughout the bulk, whereas a minor signal of Cl was identified at the film surface, indicating most of Cl was sublimated out the film during annealing (Fig.2c,d). This is in contrast to the $CsSnI_3$:$PbBr_2$ and $CsSnI_3$:PbI_2 thin films, which show a uniform distribution of Br and I from the surface to the bulk.

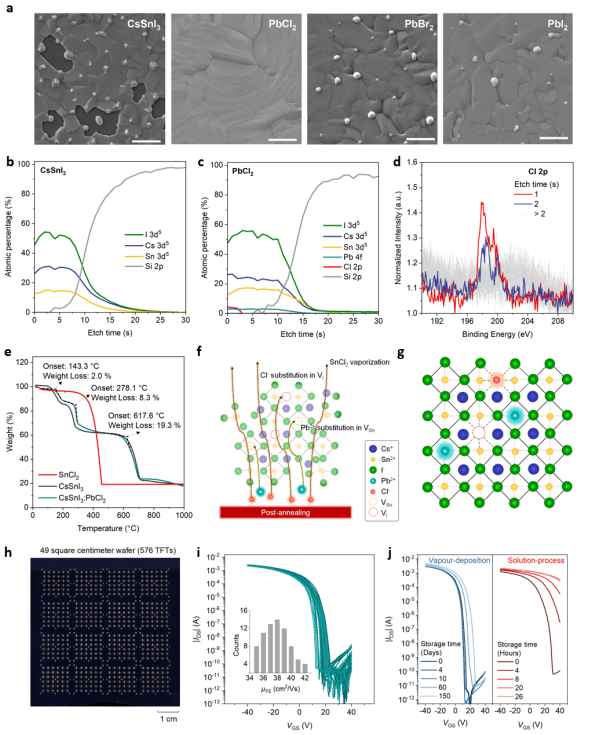

Fig. 2. a, SEM images of of $CsSnI_3$, $CsSnI_3$:$PbCl_2$, $CsSnI_3$:$PbBr_2$, $CsSnI_3$:PbI_2 thin films (scale bar: 2 μm). b,c, XPS depth analysis of deposited (b) $CsSnI_3$ and (c) $CsSnI_3$:$PbCl_2$ thin films on bare Si substrates. Etch rate is 0.5 nm/s. d, Cl 2*p* core level XPS spectra of $CsSnI_3$:$PbCl_2$ thin film with etch time = 1~30 s . e, Thermogravimetric analysis (TGA) of as-evaporated $CsSnI_3$:$PbCl_2$ thin film. f, Illustration of post-annealing treatment on $PbCl_2$ effect of evaporated perovskites. g, Schematic of final vapour-deposited $CsSnI_3$:$PbCl_2$ lattice composition. h, Image of 49 square centimeter wafer with 24 × 24 = 576 devices. Marked in yellow are 75 devices evenly selected from wafer-scale array. i, Transfer characteristics of 75 devices evenly selected from the wafer-scale array. Channel length/width = 100 μm/200 μm (V_{DS} = -40 V). Inset shows the distribution of field-effect mobilities of the evenly selected 75 TFTs. j, Current-voltage transfer curves as a function of storage time in N_2-filled glove box of (left) vapour-deposited, (right) solution-processed $CsSn_{0.9}Pb_{0.1}I_3$ TFTs without encapsulation.

To identify the form of vaporized Cl, we conducted

powder thermogravimetric analysis collected from the as-evaporated pristine $CsSnI_3$ and $CsSnI_3$:$PbCl_2$ thin films (Fig.2e). Both films demonstrate comparable trend, but a notable difference is identified between the weight loss below 100 °C, where $CsSnI_3$:$PbCl_2$ film showed 2% weight loss since the beginning. To identify the origin of this weight loss, we conducted TGA of each CsI, SnI_2, $PbCl_2$, $SnCl_2$ and CsCl powder, and only $SnCl_2$ demonstrated initial 2% weight loss, identical to $CsSnI_3$:$PbCl_2$ film. Thus, we speculate the vaporization of Cl occur in form of $SnCl_2$ during annealing. The vaporization of Cl can promote grain growth in vertical direction, promoting perovskite phase formation of sequentially deposited precursor layers and consequently enhanced film crystallinity. The residue Cl on the film surface may passivate the iodide vacancy as aligned with the positive peak shift in the XRD spectrum (Fig.2f,g). The epitome of thermal evaporation is the ease of processing and scalability of thin films and devices. We therefore demonstrate large-area fabrication of $CsSnI_3$:$PbCl_2$ TFTs on a 49 square centimeter wafer (Fig.2h). The transfer characteristics of 75 evenly selected devices out of 576 $CsSnI_3$:$PbCl_2$ TFTs show high uniformity, with a Gaussian distribution of μ_{FE} averaging 39.8 $cm^2 V^{-1} s^{-1}$ and a standard deviation of 3.5 $cm^2 V^{-1} s^{-1}$ (Fig.2i). This is the first-ever demonstration of large-scale 3D Sn^{2+}-halide perovskite TFT arrays. It should be noted that fabricating high-performance and uniform Sn^{2+}-perovskite TFTs over a large area has remained an unsolved challenge when using the typical spin-coating approach. This difficulty arises from the necessity of adding an anti-solvent dripping to promote nucleation for highly crystalline films during spin-coating, which results in varying perovskite film quality from center to edge.

More importantly, vapour-deposited $CsSnI_3$:$PbCl_2$ TFTs exhibit much improved storage stability in an N_2-filled glove box. In contrast, earlier works on solution-processed $CsSnI_3$-based perovskite TFTs could only achieve long-term stability with glass or polymer encapsulation[8]. Without encapsulation, solution-processed $CsSnI_3$ TFTs lasted only a few hours, even when stored in the glove box (Fig.2j).

3 Conclusions

We report high-performance, stable p-channel $CsSnI_3$-based TFTs utilizing a commercially compatible vapour-deposition approach. The volatile Cl triggers solid-state reactions and the conversion of as-evaporated precursor compounds. This not only facilitates the formation of high-quality and uniform perovskite films but also modulates the high hole density, making them suitable for use as channel layers. The optimized $CsSnI_3$:$PbCl_2$ TFTs deliver average μ_{FE} of ~40 $cm^2 V^{-1} s^{-1}$, I_{on}/I_{off} exceeding 10^8, and superior storage stability over 150 days. We also demonstrated a large-scale Sn^{2+}-halide perovskite TFT array that overcomes the technical challenges faced in the solution-process. Our vapour-deposited TFTs have a high potential for applications as backplane TFTs for OLED displays using the same process and as logic devices and circuits in monolithic 3D integration that require low process temperatures.

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