Monolithic 3D Integration of Vertically stacked IGZO-Te CMOS Inverter

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Keywords: M3D, CMOS, IGZO, Te

ABSTRACT

We demonstrate monolithic 3D integration of vertically stacked CMOS inverters using n-type IGZO and p-type Te TFTs. Vacuum-based fabrication ensures high-quality films, while the stacked architecture shortens interconnects and increases integration density. Compared with planar CMOS, the inverters show robust operation with a simpler process.

1 Introduction

Complementary metal-oxide-semiconductor (CMOS) inverters are implemented based on the complementary operation of p-type and n-type thin-film transistors (TFTs), and are essential for stable and low-power logic circuit design. For n-type semiconductors, relatively well-established material systems, including oxide semiconductors, have enabled attempts to fabricate inverters using only n-type TFTs. However, such structures inherently suffer from limited output swing, low input driving capability, high power consumption, and unstable noise characteristics. In contrast, stable candidates for p-type semiconductors remain scarce. Although organic semiconductors and metal chalcogenides have been investigated as alternatives, their complex fabrication processes and intrinsic limitations hinder their application to high-performance CMOS logic. Therefore, the realization of high-performance CMOS inverters requires a p-type semiconductor that simultaneously offers excellent electrical characteristics and simplified fabrication.

As Moore's law reaches its physical and process limits, three-dimensional (3D) integration has gained attention as a pathway to extend integration density beyond conventional scaling. Conventional methods, such as wire bonding and through-silicon vias (TSVs), have enabled vertical integration but suffer from process complexity, silicon-centric constraints, and additional parasitics, limiting their applicability to thin-film, display-oriented processes. Monolithic 3D (M3D) integration offers an attractive alternative by stacking devices directly, thereby shortening interconnects, reducing parasitic effects, improving energy efficiency, and enabling heterogeneous device integration.

In this work, monolithic 3D (M3D) integration of n-type IGZO and p-type Te TFTs was fabricated to realize CMOS inverters. All device layers were deposited using vacuum process, providing a simplified process while reducing interconnect length and parasitic effects, thereby enabling higher integration density and robust operation. Comparative evaluation with planar counterparts highlights both performance and manufacturability advantages, underscoring the strong potential of this approach for next-generation circuit applications.

2 Experiment

CMOS inverters were fabricated by M3D process in which a bottom n-type oxide TFT and a top p-type Te TFT were vertically stacked. Fig.1 presents the step-by-step process flow for device fabrication.

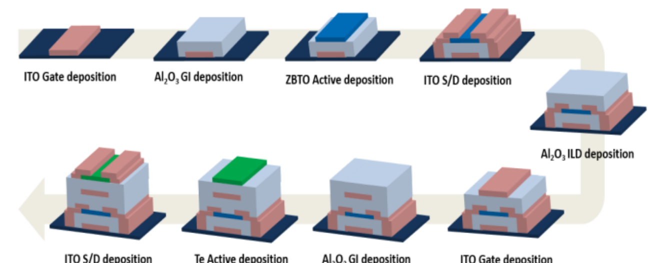

Fig. 1 Schematic illustration of the fabrication process for the vertically stacked IGZO-Te CMOS device

First, a 40nm ITO gate electrodes were deposited using a sputtering, patterned by shadow mask. Subsequently, the 55nm Al_2O_3 gate dielectric layer was deposited at 250°C using a PEALD process. Trimethylaluminum (TMA) precursor was used with O_2 plasma. PEALD cycle consisted of TMA 0.3s, Ar purge 20s, O_2 stable 3s, O_2 plasma 1s, and Ar purge 5s. Here, Al_2O_3 was patterned by conventional photolithography process followed by lift-off process. The Al_2O_3 layer was subjected to rapid thermal annealing (RTA) at 300°C for 1h in air. Subsequently, a 20nm IGZO channel layer was deposited using a radio frequency (RF) sputtering process (Ar: 10sccm, working pressure: 3mtorr, RF power: 80W), and the channel area was defined by shadow mask. The IGZO layer was annealed by RTA in air at 350°C for 1h. Subsequently, a 50nm ITO S/D layer was deposited by the magnetron sputtering process, also patterned by shadow mask. The 55nm Al_2O_3 inter

layer dielectric (ILD) was deposited at 150°C using a PEALD process. The Al_2O_3 ILD was optimized to suppress degradation of the bottom channel and to electrically/physically isolate the top and bottom TFTs, thereby minimizing inter-tier interference. a 40nm ITO gate electrodes were deposited using a sputtering. An additional 55nm Al_2O_3 layer was deposited by PEALD on the top-gate electrode to serve as the gate dielectric for the Te TFT. Subsequently, a 15nm Te channel layer was deposited using a RF sputtering process (Ar: 10sccm, working pressure: 3mtorr, RF power: 20W), and the channel area was defined by shadow mask. The Te layer was annealed by RTA in air at 150°C for 1h. Subsequently, a 50nm ITO S/D layer was deposited by the magnetron sputtering process.

3 Results

Prior to full M3D fabrication, we characterized and optimized the PEALD Al_2O_3 employed both as the gate dielectric and the interlayer dielectric (ILD). In vertically stacked devices, upper-layer depositions can perturb the bottom-tier TFT; without proper optimization, we observed degradation arising from residual $–CH_x$/–OH ligands of the TMA precursor and from plasma-induced interactions that modify channel doping and trap states. A moderate incorporation of hydrogen-related species can transiently passivate traps and enhance mobility and on-current, but excessive hydrogen creates defect states and accelerates instability. To regulate these effects, the O_2 plasma power during PEALD was systematically varied (50, 70, and 100 W, properties of Al_2O_3 with 50, 100 W power are not shown in here). At low plasma power, incomplete reactions left residual ligands, degrading dielectric quality and increasing leakage, while also causing partial oxidation of the active layer. Conversely, high plasma power improved dielectric density but generated excess interstitial oxygen, which diffused into the channel during annealing. Although some oxygen vacancies were compensated, overly strong plasma conditions damaged the underlying TFT, worsening electrical stability. An intermediate plasma power of 70 W provided the most balanced outcome, producing Al_2O_3 films with a dielectric constant of ~8.31 and a breakdown field of over 6 MV/cm, while minimizing hydrogen incorporation and preventing degradation of the bottom tier during subsequent stacking, as shown in **Figure. 2**. These optimized Al_2O_3 layers thus provide both high dielectric performance and structural robustness, enabling reliable operation of M3D-integrated TFTs.

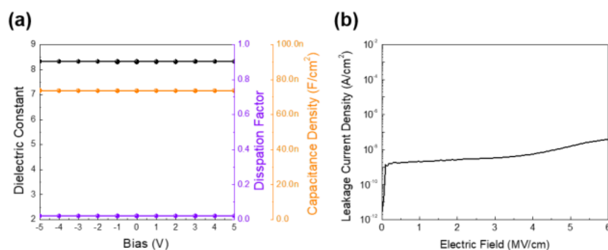

Fig. 2 Electrical properties of PEALD-deposited Al_2O_3 dielectric: (a) dielectric constant, dissipation factor, and capacitance density as a function of bias voltage, (b) leakage current density versus electric field

The transfer characteristics of the bottom-layer IGZO TFT were examined at successive fabrication stages, including the bare device, after ILD deposition, after top gate and gate insulator formation, after Te channel deposition, and finally after the top source/drain electrodes. **Figure 3.** shows the transfer curve of the bottom layer IGZO TFT in the vertical stack configuration. Fig3 (a) presents the transfer curve of the bottom layer TFT without the overlying layers, while Fig3 (b) shows the curve after fabrication of M3D, while others are not included for clarity. Before deposition of the overlying layers, the IGZO TFT exhibited a mobility of 18.14 cm^2/Vs, a V_{th} of -0.67 V, and a SS of 0.11 V/dec, whereas after fabrication of M3D, it showed a mobility of 19.09 cm^2/Vs, a V_{th} of -1.53 V, and a SS of 0.12 V/dec. As stacking proceeded, slight variations in the electrical characteristics were observed during the layer stacking and subsequent annealing process, but no significant degradation was detected. The variations in electrical characteristics with respect tot each layer stacking condition are summarized in the **table1**. The results indicate that even after stacking, the bottom layer TFT maintains its performance without significant degradation.

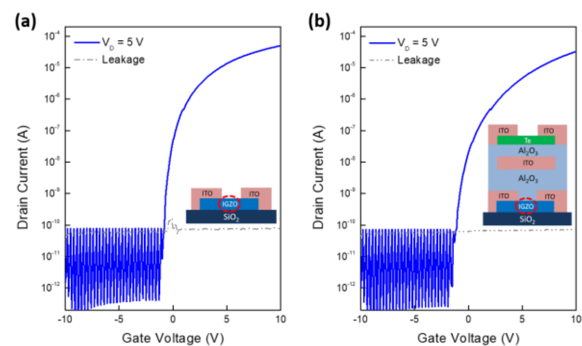

Fig. 3 Transfer characteristics of IGZO TFTs (V_D = 5 V): (a) before stacking, showing the initial TFT performance, (b) after stacking, exhibiting the electrical behavior of the vertically integrated structure.

Table 1.

	Bare	After ILD	After Top Gate	After Top GI	After Te	After Top S/D
μ_{FE}(cm^2/Vs)	18.14	15.28	19.33	20.09	20.96	19.09
V_{th} (V)	-0.67	-0.07	-3.04	-0.43	-0.40	-1.53
SS (V/dec)	0.11	0.12	0.16	0.07	0.08	0.12

Figure 4. shows the transfer and output curve of the top layered Te TFT in the vertical stack configuration. The vertically stacked Te TFT exhibited stable p-type operation with a mobility of 6.15 cm^2/Vs, and a SS of 1.31 V/dec, demonstrating that the IGZO layer retained high device performance even after integration of the upper stack. The output characteristics confirmed well behaved p-type conduction under negative gate bias with ohmic like contact. Furthermore, AFM analysis in Fig3 (c) and (d) revealed a smooth Te surface with RMS roughness values below 1nm (0.56nm on SiO_2 and 0.67nm on Al_2O_3), indicating high film quality suitable for stacked device favrication.

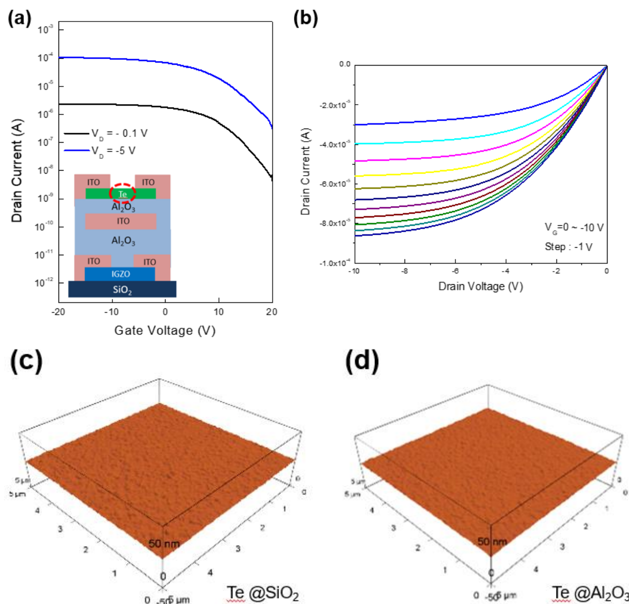

Fig. 4 Electrical and morphological characteristics of vertically stacked Te TFT: (a) transfer characteristics and (b) output characteristics. AFM images of Te thin films deposited on (c) SiO_2 and (d) Al_2O_3.

By integrating a bottom IGZO TFT and a top Te TFT in a monolithic 3D stacked configuration, we successfully fabricated a CMOS inverter. The trasfer curves exhibited well-defined switching behavior under V_{DD} ranging from 2 to 10 V, demonstrating stable CMOS operation. The output swing increased with higher V_{DD}, confirming proper complementary operation of the vertically stacked devices. Corresponding gain characteristics revealed a high gain of approximately 25 at V_{DD} of 10 V, indicating sharp switching and strong signal amplification. These results highlight that the proposed M3D inverter structure not only maintains reliable functionality of both the bottom and top TFTs after stacking, but also achieves high gain performance, thereby validating its potential for high-density, low-power circuit applications.

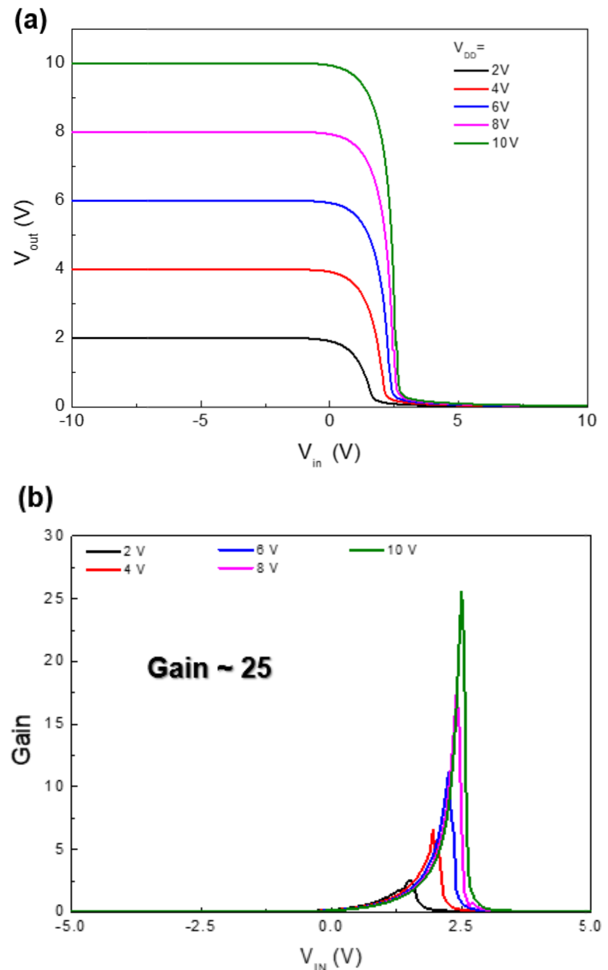

Fig. 5 Electrical characteristics of the M3D CMOS inverter: (a) voltage transfer curves at different supply voltages, (b) corresponding voltage gain curves

4 Conclusions

In this work, we demonstrate a monolithic 3D CMOS inverter composed of a bottom-layer IGZO TFT and a top-layer Te TFT. The integration flow was optimized by tuning the dielectric properties of PEALD Al_2O_3 and adjusting plasma conditions, thereby minimizing degradation of the bottom device during stacking and passivation. In the vertical configuration, the Te TFT maintained stable p-type operation, while the IGZO TFT preserved its n-type characteristics, enabling robust complementary logic. The fabricated CMOS inverter exhibited well-defined voltage transfer characteristics with a maximum gain of 25 under V_{DD} ranging from 2 to 10 V, confirming reliable high-performance operation. These results underscore the promise of M3D integration as a pathway toward high-density, low-power oxide-based circuits for next-generation display and electronic systems.

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