High-Performance p-type Tellurium-Selenium Oxide Thin-Film Transistors Fabricated by Sputtering

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ABSTRACT

In the study, high-performance p-type Te_xSe_yO *thin-film transistors were fabricated by RF magnetron sputtering, enabling superior film quality.* Al_2O_3 *layer was employed as high-k gate dielectric for low-power operation and passivation. The devices exhibited enhanced mobility, improved on/off current ratio, and significantly better long-term stability compared with conventional p-type Te transistors.*

1 Introduction

The advancement of modern electronics technologies, particularly for large-area applications such as displays and sensor arrays, heavily relies on the development of high-performance and low-cost thin-film transistors (TFTs). While n-type amorphous oxide semiconductors, represented by amorphous indium-gallium-zinc oxide (a-IGZO), have achieved excellent performance and commercialization as key channel materials for display industries. However, the lack of comparable p-type oxide semiconductors limits the realization of fully complementary metal-oxide-semiconductor (CMOS) circuits. Existing p-type oxides exhibit low mobility, high off current, poor environmental stability, complex fabrication processes, and high processing temperatures, which hinder performance improvements and make CMOS implementation challenging.

Tellurium-based oxides have emerged as promising p-type channel materials due to their unique electronic structure originating from Te 5p orbitals, which can form a delocalized valence band maximum (VBM). However, pure tellurium oxides face challenges in achieving both high mobility and stability, due to intrinsic defect states and suboptimal band structure alignment. Additionally, their inherently narrow bandgap leads to high off-current, making it difficult to attain a sufficient on/off current ratio. Recent studies have suggested that doping the tellurium oxide matrix with selenium to form tellurium-selenium oxides (Te_xSe_yO) can effectively modulate material properties. Selenium alloying is expected to suppress defect states, tune the bandgap and VBM energy levels, and enhance p-orbital connectivity, thereby providing a pathway to superior electrical performance.

Despite the potential of Te_xSe_yO, previous studies have largely relied on thermal evaporation, which faces challenges in achieving precise stoichiometric control over large-area deposition and often fails to produce uniform, high-density films required for high-performance devices. In contrast, radio-frequency (RF) magnetron sputtering allows more flexible control of film composition and provides superior thickness uniformity and film density across large substrates, making it particularly suitable for scalable manufacturing. At the same time, it promotes film growth and enhances adhesion, ensuring reliable device operation.

In this study, high-performance p-type Te_xSe_yO thin-film transistors were realized using RF magnetron sputtering. Key process parameters, including sputtering power, gas flow, and oxygen partial pressure, were systematically optimized to precisely control the selenium content, resulting in enhanced crystallinity, uniform surface morphology, and dense microstructure. A high-k Al_2O_3 gate dielectric was also employed for low-power operation, as its larger capacitance at a given thickness enables stronger gate control and reduced operating voltage. Also, Al_2O_3 was deposited as a passivation layer to protect the Te_xSe_yO channel from environmental degradation and improve device stability. The fabricated Te_xSe_yO TFTs demonstrated mobility and on/off current ratios compare to conventional p-type Te TFTs, along with significantly improved long-term stability. These results indicate that Te_xSe_yO can mitigate the intrinsic electronic-structural limitations of p-type oxide semiconductors, establishing it as a promising material platform for next-generation oxide CMOS circuits and large-area, low-cost electronic devices.

2 Experiment

A 55 nm-thick Al_2O_3 gate dielectric was deposited by plasma-enhanced atomic layer deposition (PEALD) using trimethylaluminum (TMA) as the precursor and oxygen plasma as reactant. Post-deposition thermal annealing was carried out at 300 °C for 1 hour in ambient to stabilize the dielectric properties. A 15 nm-thick tellurium–selenium channel layer was subsequently deposited by RF magnetron sputtering at a plasma power of 40 W and a process pressure of 10 mTorr, conditions optimized to achieve uniform thickness and stable composition. The as-deposited films were then subjected to post-annealing at 200 °C for 1 hour in air to improve their structural and electrical properties. Source/drain electrodes of 100 nm-thick Ni were

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deposited by thermal evaporation. To further investigate the passivation effect, photolithography and lift-off was employed, followed by the deposition of Al_2O_3 passivation layers with thicknesses ranging from 5 to 20 nm via PEALD. Subsequent thermal annealing was performed at 150 °C for 1 hour in ambient air. The electrical characteristics of the fabricated TFTs were evaluated using a Keithley 4200A-SCS semiconductor characterization system in dark, ambient.

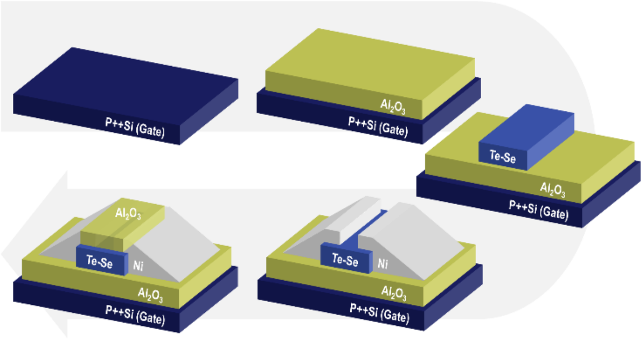

Fig. 1 Fabrication process flow of Te_xSe_yO TFTs.

3 Results and Discussion

Al_2O_3 thin films were deposited via PEALD, and their applicability as gate dielectrics was evaluated. The deposited Al_2O_3 films exhibited excellent dielectric and electrical properties. Figure 2 shows the electrical and dielectric properties of Al_2O_3 fabricated by PEALD. Fig. 2a shows the capacitance-voltage (C-V) curves measured at 100 kHz. High dielectric constant of 8.9 provide high capacitance density advantageous for scaling in next-generation devices. Electrical properties was assessed through current-voltage (J-V) curve as shown in Fig. 2b. The leakage current density remained low over the entire applied electric field range, exhibiting values below 10^{-9} A/cm^2 at 1 MV/cm. Furthermore, the breakdown field (E_{break}) was over 8 MV/cm, confirming the excellent insulating characteristics. The combination of low leakage current and high breakdown field highlights the strong insulating properties of the oxide films. In addition, the films exhibited a low density of electron traps, thereby reducing charge trapping and enhancing device stability. Owing to their excellent thermal and chemical robustness, Al_2O_3 films deposited by PEALD show great promise as gate dielectric materials for next-generation semiconductor devices.

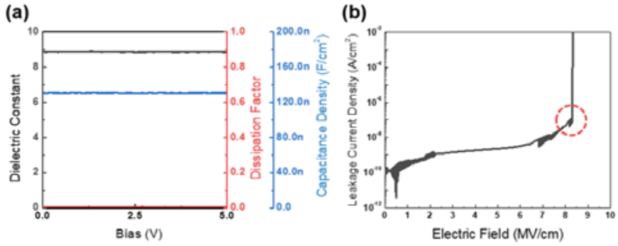

Fig. 2 Dielectric and electrical characteristics of PEALD-deposited Al_2O_3. (a) Figure showing dielectric constant and capacitance density. (b) Figure showing the leakage current and breakdown field.

The electrical characteristics of Te_xSe_yO channel layers with various thicknesses of 10, 15, and 20 nm were systematically investigated. Fig. 3 shows the transfer characteristics of Te_xSe_yO TFTs with various thicknesses, and the corresponding representative parameters are summarized in Table 1. The 10 nm-thick device exhibited low mobility, pronounced hysteresis, and relatively reduced on- and off-current levels compared with the other Te_xSe_yO TFTs, as shown in Fig. 3a. As the channel thickness increased to 15 nm, the TFT exhibited a higher on-current as well as a higher off-current, while maintaining an on/off ratio comparable to that of the 10 nm-thick Te_xSe_yO TFT, as shown in Fig. 3b. In Fig. 3c, the 20 nm thick Te_xSe_yO TFT exhibited a significant increase in mobility and on-current; however, the off-current also rose notably, resulting in a degraded on/off ratio. "Despite the thickness variation, all three devices commonly exhibited low mobility, large hysteresis, and limited on/off current ratios, which can be attributed to the intrinsic instability of the tellurium–selenium channel, including charge trapping effects caused by interface defects, surface oxidation, and external contamination.

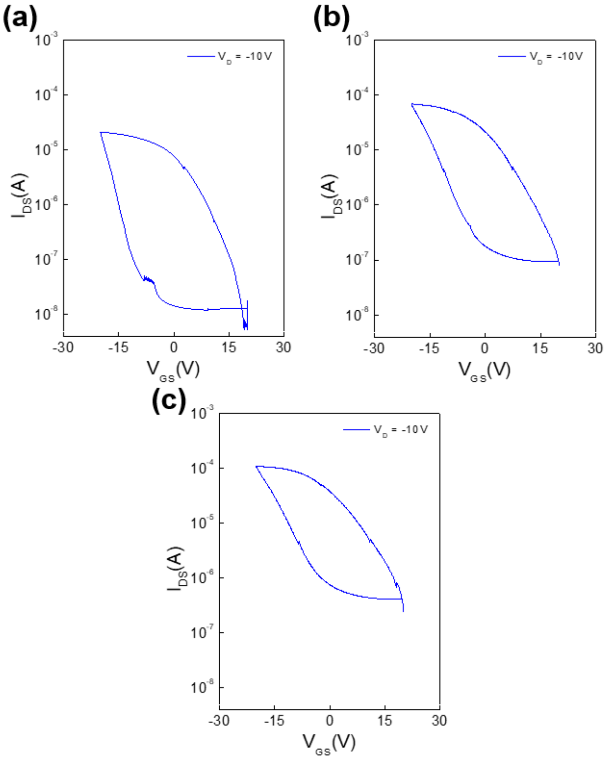

Fig. 3 Transfer curves of Te_xSe_yO TFTs with different channel thicknesses of (a) 10 nm. (b) 15 nm. (c) 20 nm.

Tellurium–selenium channels are highly susceptible to interface defects, surface oxidation, and ambient contamination, which induce charge trapping and degrade device performance. To mitigate these issues, Al_2O_3 passivation layers were introduced, and the electrical characteristics were systematically analyzed with different passivation thicknesses of 5, 10, and 20 nm at Te_xSe_yO channel thickness of 15 nm and 20 nm, which were selected as representative conditions: 15 nm for its balanced mobility–leakage characteristics and 20 nm for its highest mobility prior to passivation. Fig. 4 shows the transfer curves of Te_xSe_yO TFTs with 15 and 20 nm channel thicknesses under various passivation thicknesses and their transfer parameters are summarized in Table 2. Both Te_xSe_yO TFTs with 15 and 20 nm channel layers exhibited a significant reduction in hysteresis and off-current after passivation. For the 20 nm Te_xSe_yO channel, the device performance showed little variation with passivation thickness, although the best results were obtained with a 10 nm passivation layer (Fig. 4b). In contrast, the 15 nm channel devices exhibited a pronounced dependence on passivation thickness, with all passivation layers significantly reducing the off-current. However, while the 5 and 10 nm passivation layers also caused a considerable decrease in the on-current, the 20 nm passivation layer maintained a low off-current while preserving a high on-current, as shown in Fig. 4a.

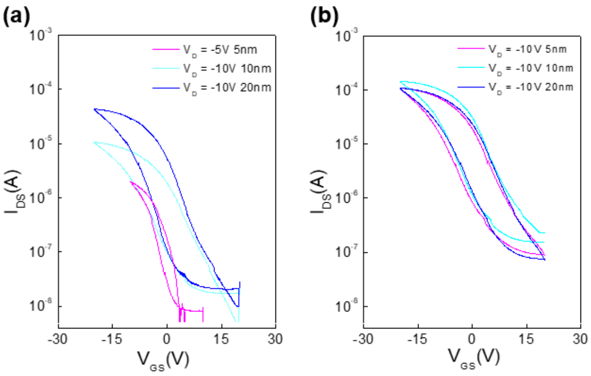

Fig. 4 Transfer curves of Te_xSe_yO TFTs passivated with Al_2O_3 of different thicknesses. With a channel thickness of (a) 15 nm. (b) 20 nm.

Table 1. Electrical parameters of Te_xSe_yO TFTs before Al_2O_3 passivation.

Channel thickness	Mobility (cm^2/Vs)	Hysteresis (V)	Swing (V/dec)	$I_{on/off}$
10 nm	0.40	25.60	1.26	$4.57x10^3$
15 nm	1.93	19.60	2.72	$8.76x10^2$
20 nm	2.53	19.90	1.96	$4.37x10^2$

Table 2. Electrical parameters of Te_xSe_yO TFTs after Al_2O_3 passivation.

Channel thickness	Passivation thickness	Mobility (cm^2/Vs)	Hysteresis (V)	Swing (V/dec)	$I_{on/off}$
15 nm	5 nm	0.09	3.14	0.85	$1.53x10^3$
	10 nm	0.20	9.00	1.61	$2.18x10^3$
	20 nm	3.71	8.56	1.49	$4.43x10^3$
20 nm	5 nm	2.59	9.56	4.16	$1.25x10^3$
	10 nm	3.10	9.74	4.18	$6.53x10^2$
	20 nm	2.61	8.78	4.21	$1.52x10^3$

The output characteristics were analyzed to confirm channel control, contact resistance, and current-driving capability through the distinction between the linear and saturation regimes, and all devices exhibited ohmic contacts. For the comparison devices with a SiO_2 gate insulator, the saturation region was poorly defined (Fig. 5a). In contrast, devices employing Al_2O_3 as the gate insulator with additional passivation exhibited well-defined linear and saturation regions (Fig. 5b, c). This improvement can be attributed to the high dielectric constant of Al_2O_3, which enables the gate to more effectively control of the channel charge by the gate, and to the low trap density at the oxide/channel interface, which stabilizes charge transport and current flow.

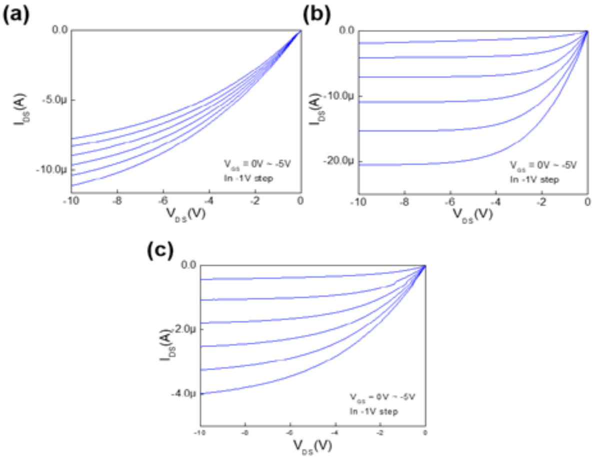

Fig. 5 Output curves of Te_xSe_yO TFTs at each fabrication step. (a) With SiO_2 gate insulator. (b) With Al_2O_3 gate insulator. (c) With Al_2O_3 gate insulator and passivation.

4 Conclusions

In this study, we demonstrate tellurium–selenium thin-film transistors (TFTs) designed for low-power operation by employing a high-k Al_2O_3 layer as the gate dielectric and passivation layer. The Te_xSe_yO channel layer was deposited by RF magnetron sputtering, yielding uniform and high-quality thin films. A representative Te_xSe_yO device with a 15 nm channel layer and a 20 nm Al_2O_3 passivation layer exhibited excellent electrical performance, including a field-effect mobility of 3.71 $cm^2/V\cdot s$, a hysteresis window of 8.56 V, a subthreshold swing of 1.49 V/dec, and an on/off current ratio of 4.43×10^3. These results highlight the promise of the Te_xSe_yO material system for integration into next-generation oxide CMOS circuits as well as large-area, low-cost electronic applications.

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