Recent advances in LTPO technology for mobile OLED Displays

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ABSTRACT

This research introduces an innovative 3D-structured complementary metal-oxide-semiconductor (CMOS) inverter, alongside its integration into narrow-bezel AMOLED displays, leveraging the advanced capabilities of low-temperature polycrystalline silicon and oxide thin-film transistors (LTPO TFTs). By vertically aligning an n-type oxide TFT on a p-type LTPS TFT without additional photo masks, the circuit area is reduced from 1,581 μm² to 775 μm². The vertical CMOS inverter features a dual gate structure, enhancing the oxide TFT's performance and stability, with improved voltage gain (113.0 to 140.2 V/V). Positive bias stress stability of the vertical CMOS inverter was improved, resulting in the decrease of voltage transfer curve shift from 0.63 to 0.25 V. Based on the 3D-structured CMOS inverter circuit proposed, the new LTPO gate driver in panel (GIP) circuit reduces the GIP size by approximately 20%. The proposed inverter circuit structure and its application to the GIP demonstrate the potential for reducing bezel size, offering promising benefits for future applications.

1 Introduction

In recent years, active-matrix organic light-emitting diode (AMOLED) display backplane technology has evolved from low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs) to low-temperature polycrystalline silicon and oxide thin-film transistors (LTPO TFTs) [1], [2]. The LTPO backplane-based pixel compensation circuit has emerged as the predominant configuration in AMOLED displays. It is noteworthy that the LTPO pixel compensation circuit exhibits a higher degree of complexity relative to its LTPS counterpart, primarily attributed to the necessity of incorporating low refresh rates to achieve enhanced power efficiency. As a result, multiple GIPs drivers are required to drive the pixels in a display. [3], [4].

In the view of an inverter which is a basic logic gate of GIP, LTPO technology with complementary metal oxide (CMOS) logic allowed the inverter to exhibit wider output voltage swings, higher voltage gain, and lower power consumption than a pseudo-NMOS inverter. In this sense, LTPO technology has expanded its applicability from compensation circuits to GIPs [5]. In the previous researches on LTPO TFT-based inverters, it was observed that these inverters predominantly utilized a conventional planar structure, wherein the LTPS and oxide thin-film transistors (TFTs) were arranged horizontally [6], [7]. From the perspective of gate driver in panel (GIP), this planar configuration has a limitation in that it increases the area occupied by the GIP, thereby enlarging the bezel area. For the latter limitation, otherwise it causes the problem that induces a lower voltage gain and changes the voltage range defining high and low logic states under continuous pulse stress. Thus, a structural approach is required to reduce the area occupied by the inverter while improving the performance of the oxide TFT.

In this study, a vertical CMOS inverter using LTPO TFT is proposed for narrowing the bezel area, improving electrical performance and stability. The vertical CMOS inverter is composed of LTPS and oxide TFT that have gate electrodes aligned in the same position vertically. The oxide TFT in the vertical CMOS inverter has a dual gate structure to improve electrical performance and stability against positive bias stress (PBS). To confirm whether the bezel area can be reduced by using the vertical CMOS inverter, the effective circuit area is compared between the planar and vertical CMOS inverter from the real image of the fabricated devices. To compare the electrical performance and stability of both inverters, the transfer characteristics of the LTPS and oxide TFT and the voltage transfer curve (VTC) of both inverters are measured.

Also, based on the proposed 3D-structured CMOS inverter, we have proposed and validated an applicable LTPO GIP circuit. By applying the 3D-structured CMOS inverter to the new LTPO GIP circuit, the GIP size is dramatically reduced. The proposed inverter circuit and its application to the GIP show potential for reducing bezel size. These innovations not only reduce the bezel area but also enhance the efficiency and stability of AMOLED display backplanes.

2 Experiment

This research focuses on enhancing the performance and reducing the size of GIP circuit used in AMOLED displays. The study introduces a vertical CMOS inverter utilizing LTPS and oxide TFT as an alternative to conventional planar CMOS inverters.

The fabrication process for LTPS TFT and oxide TFT in the planar CMOS inverter involves depositing an amorphous silicon (a-Si) layer on a polyimide (PI) substrate using plasma-enhanced chemical vapor deposition (PECVD). The a-Si layer is then crystallized via excimer laser annealing (ELA) to form the LTPS channel. A silicon oxide (SiO_2) gate insulator is deposited, followed by the formation of a molybdenum (Mo) gate electrode for the LTPS TFT. For the oxide TFT, an indium-gallium-zinc oxide (IGZO) channel is deposited using a sputtering method. The fabrication process for the vertical CMOS inverter is identical to that of the planar CMOS inverter, ensuring consistent performance and area comparison.

Furthermore, by employing vertically structured CMOS inverter circuits, significant reductions in the GIP footprint can be achieved. This research proposes innovative methodologies in GIP circuit design utilizing vertical CMOS inverters, with the primary goals of minimizing bezel dimensions and enhancing the stability of AMOLED displays.

3 Results

To demonstrate the structure of planar and vertical CMOS inverters, cross-sectional and OM images of the top views of inverters composed of LTPS and oxide TFTs were presented in Fig. 1a-d. Focused ion beam (FIB) images were shown in parts a and c. In the FIB image, the gate electrodes of the LTPS and oxide TFTs were labeled as "gate" to determine whether the gate electrodes are utilized independently or shared. As depicted in Fig. 1a, the planar CMOS inverter employed a horizontally arranged structure of LTPS and oxide TFTs, featuring a single top gate electrode for each. Conversely, the vertical CMOS inverter utilized a vertically arranged structure of LTPS and oxide TFTs, sharing the top gate electrode of the LTPS TFT with the oxide TFT. Given that the oxide TFT has an additional top gate electrode, it exhibited a dual-gate structure. To confirm whether the effective circuit area of the fabricated inverter is reduced by using the vertically arranged structure, optical micrograph (OM) images of the planar and vertical CMOS inverter were shown in Fig. 1b and d, respectively. In Fig. 1b and d, the highlighted white solid-line area is the effective circuit area covering a channel, a gate, and source/drain metal electrodes. Due to the vertically arranged structure, the effective circuit area is reduced from 1,581 to 775 μm^2.

Electrical characteristics of the TFTs including linear mobility (μ), threshold voltage (V_{TH}), and subthreshold slope (SS) are summarized in Table 1. The LTPS TFTs showed consistent electrical characteristics due to the same fabrication process regardless of the structure of the inverters. On the other hand, the oxide TFT of the vertical CMOS inverter is improved compared to that of

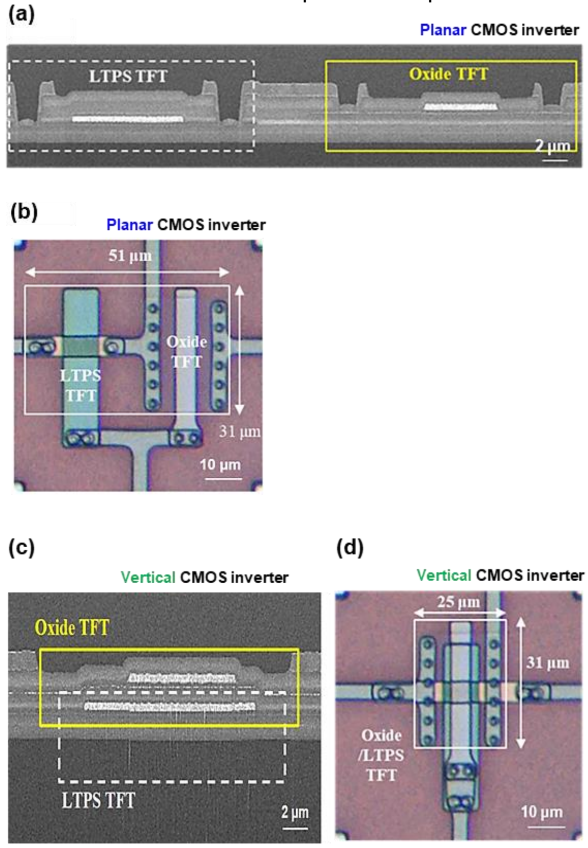

Fig. 1. (a) FIB image of the cross-sectional view and (b) OM images of the top view of the planar and (c) FIB image of the cross-sectional view and (d) OM images of the top view of the vertical CMOS inverter.

the planar inverter. This is because the oxide TFT of the vertical CMOS inverter has a dual-gate structure. In the vertical CMOS inverter, the SS and μ of the oxide TFT are improved by the increased effective channel thickness due to the additional electric field induced by the bottom gate bias [8]. Fig. 2 shows the VTCs which plot the output voltage (V_{OUT}) against the input voltage (V_{IN}) and voltage gain curves of the planar and vertical CMOS inverter where the V_{IN} is from 1.2 V to 2.0 V. The VTC of the vertical CMOS inverter is shifted negatively about 0.2 V compared to the planar inverter. It is because the drain current of the oxide TFT of the vertical CMOS inverter is larger than that of the planar CMOS inverter [9], [10]. The voltage gain ($|dV_{OUT}/dV_{IN}|$) of the vertical CMOS inverter is improved from 113.0 to 140.2 V/V. Fig. 3a and b showed positive bias stress (PBS) test results of the oxide TFT in the planar and vertical CMOS inverter applying positive unipolar gate pulse with a pulse amplitude of 5 V, a pulse width of 20 μs, and a duty ratio of 50%, respectively. The test was performed at room temperature for 500 hours operation. The transfer curve of the oxide TFT in the vertical CMOS inverter. showed improved PBS stability with the positive V_{TH} shift from 1.2 to 0.6 V. It is because the electron trapping at the interface between channel and gate insulator is

TABLE I. Electrical Characteristics of the LTPS and Oxide TFTs of the Planar and Vertical CMOS Inverter.

	Planar CMOS inverter		Vertical CMOS inverter	
Active layer	LTPS	IGZO	LTPS	IGZO
μ (cm^2/Vs)	111.01	5.55	111.02	7.75
V_{TH} (V)	-3.41	1.37	-3.35	1.02
SS (V/dec)	0.36	0.08	0.36	0.03

suppressed by the reduced vertical electric field as the gate biases interfered each other [11], [12], [13]. The PBS test results in the view of the VTCs of both inverters were shown in Fig. 3c and d.

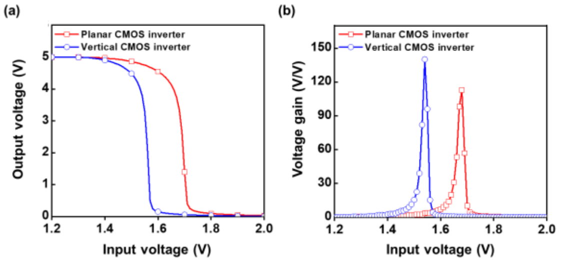

Fig. 2. (a) VTCs and (b) voltage gain curves of the planar and vertical CMOS inverter.

The PBS test was performed applying a positive unipolar pulse to input voltage with a pulse amplitude of 5 V, a pulse width of 20 μs, and a duty ratio of 50% at VDD = 5 V and VSS = 0 V. The VTCs of the planar and vertical CMOS inverters are positively shifted by 0.63 and 0.25 V, respectively.

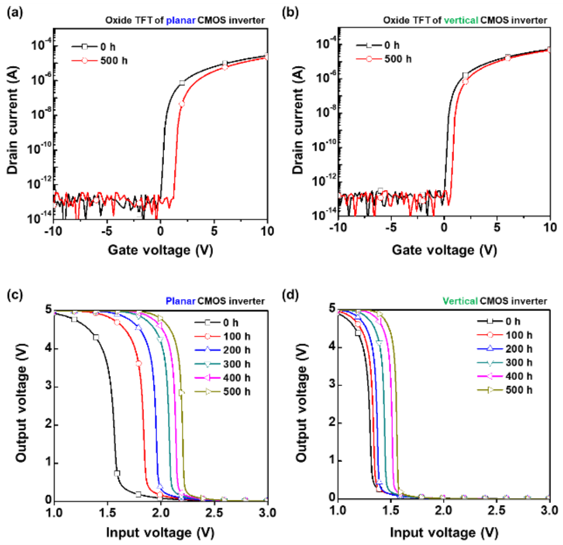

Fig. 3. Transfer curve of the oxide TFT in (a) the planar and (b) the vertical CMOS inverter and VTCs of (c) the planar and (d) the vertical CMOS inverter under PBS test with 500 hours.

Figure 4 shows a LTPO GIP circuit that can be applied to a display using the previously proposed vertical CMOS inverter. If the CMOS inverter area of this circuit is laid out using a vertical CMOS structure, the GIP size can be reduced by approximately 20% compared to the GIP size when a planar CMOS inverter structure is applied.

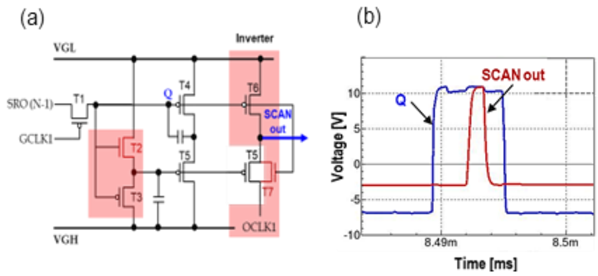

Fig.4. (a) 3D-structured CMOS inverter circuit applied to LTPO GIP circuit and (b) simulation result of LTPO GIP ouput.

4 Conclusions

In this work, the CMOS inverter using LTPO TFTs with a vertically aligned structure is proposed for reducing bezel area and improving electrical performance and PBS stability. The effective circuit area is reduced about 51% by fabricating the oxide TFT on the vertically aligned position of the LTPS TFT. The oxide TFT of the vertical CMOS inverter exhibited improved electrical characteristics such as μ from 5.55 to 7.75 cm^2/Vs, and SS from 0.08 to 0.03 V/dec. Also, the vertical CMOS inverter showed improved voltage gain from 113.0 to 140.2 V/V and PBS stability with the VTC shift from 0.63 to 0.25 V. Currently, LTPO technology is mainly used for AMOLED pixel circuit in display, but this paper presents the possibility of using it for peripheral circuits such as GIP. By applying the newly proposed 3D structure CMOS inverter to the newly proposed GIP circuit, the GIP size was reduced by approximately 20%. In addition, since a CMOS inverter is a basic unit of circuit configuration, the proposed inverter can also be used in both display and semiconductor circuits.

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