Recent Studies on Device Modeling of Oxide Semiconductor TFTs

Katsumi Abe

katsumi.abe@silvaco.com
Silvaco Japan Co., Ltd., Yokohama Landmark Tower 36F, 2-2-1 Minatomirai, Nishi-ku, Yokohama-shi, Kanagawa, 220-8136, Japan
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ABSTRACT

This paper discusses device models to predict the electrical characteristics of oxide semiconductor thin-film transistors (OS TFTs) with a dual-gate structure, a bilayer channel, and under positive-bias stresses. Device simulations using the appropriate device models can readily describe the operations and mechanisms of these OS TFTs.

1 Introduction

Oxide semiconductor thin-film transistors (OS TFTs) have been widely studied since amorphous In–Ga–Zn–O (a-IGZO) TFTs were reported in 2004 [1] because of their high field-effect mobility, low OFF current, and low process temperatures. Numerous applications using OS TFTs, including display backplanes, solar cells, gas sensors, and memory circuits, have been proposed. Recently, TFTs with a very thin OS channel fabricated by atomic layer deposition have shown promise as the upper-layer transistors in 3D integrated devices [2].

The properties of OSs affect the electrical characteristics of OS TFTs. OSs possess high Hall mobility and favorable band structure including wide bandgap (E_g) and low density of subgap states (DOSs) near the bottom of the conduction band. In addition, the good interface between the OS and gate oxide insulator, e.g., silicon oxide or aluminum oxide, allows the TFT field-effect mobility to be comparable to the OS Hall mobility. Device simulators [3,4] are available to analyze the relationships between TFT electrical characteristics and OS properties through modeling and to evaluate the effects of TFT structure on electrical characteristics. We previously developed a standard OS TFT model that was used to reproduce the dependence of TFT characteristics on temperature, channel length, and channel width via device simulations [5].

Recently, TFT structures with dual gates (DGs) and stacked channels have been studied with the aim of enhancing current capability and stability. Moreover, interest in the bias stress reliability characteristics of TFTs has increased from a device application perspective. Here we discuss device models for a DG TFT [6], a bilayer-channel TFT with a channel composed of OSs that are stable and unstable toward negative-bias temperature stress (NBTS) [7], and the positive-bias temperature stress (PBTS) reliability of OS TFTs [8]. A back-gate (BG) voltage V_{BG} can be used to control the threshold voltage V_{TH} of DG TFTs. The device simulation accurately describes the measured V_{BG} dependence of threshold voltage. Changes in the field-effect mobility of the bilayer-channel TFT under NBTS are explained by a carrier doping model for the NBTS-unstable OS. An interface trap model that considers the effects on the electric field can reproduce stretched exponential shifts of V_{TH} under PBTS.

2 Standard Device Model

As discussed in our previous report [5], the ON operation and subthreshold operation of OS TFTs are dominated by the OS drift mobility and DOSs. For OS TFTs with standard electrical characteristics, e.g., field-effect mobility exceeding 10 cm^2/(Vs) and a subthreshold swing of 0.1 - 0.4 V/dec, the OS drift mobility can be approximated using an empirical mobility model with a carrier-electron density dependence of

$$\mu_e = \mu_0 \left(\frac{N_e}{N_{CR}}\right)^{(T_\gamma/T+\gamma_0)/2} \quad (1)$$

where N_e is the carrier-electron density, T is the temperature, μ_0 represents the drift mobility of the degenerate states, N_{CR} is the critical carrier-electron density, and γ_0 and T_γ are the model parameters for the temperature dependence. The DOSs was estimated, revealing that the shallow state density near the bottom of the conduction band E_C is below 10^{20} 1/(cm^{3}eV) and the deep state density at approximately 0.3 eV from E_C ranges between 10^{17} and 10^{18} 1/(cm^{3}eV). Device simulations using the models described above can reproduce the electrical characteristics of a-IGZO TFTs, including their dependences on temperature, channel-length, and channel-width [5].

3 Structure Effects and Reliability

3.1 Dual-Gate Structure

The DG structure has two gate insulators and two gate electrodes (i.e., the gate and BG) facing each other across the OS channel. When the same voltage is applied to both gate electrodes, the subthreshold swing is smaller and the drain current I_D is higher than those of

the corresponding conventional single-gate TFT. Moreover, V_{BG} can be used to control V_{TH}, which is defined here as the gate voltage V_G at an I_D of 10^{-10} A.

A device simulation using the standard device model was performed to analyze the operation of an OS TFT with a DG structure. Fig. 1 (a) shows the structure of a DG a-IGZO TFT and Fig. 1 (b) presents measured and calculated transfer curves of the DG TFT at drain voltage V_D of 12 V and V_{BG}=-10, -5, 0, 5, and 10 V. The calculated transfer curve at each V_{BG} overlaps with the measured one. This result indicates that the device simulation with the standard device model can describe the electrical characteristics of the DG a-IGZO TFT over the wide bias range between subthreshold operation and ON operation. The device simulation is therefore suitable to consider operation mechanisms of this DG OS TFT.

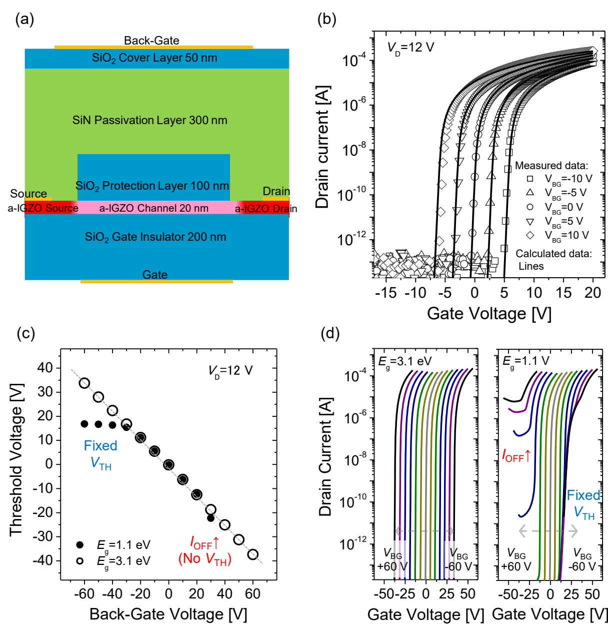

Fig. 1 (a) Structure of a DG a-IGZO TFT. (b) Transfer curves at V_D=12 V and V_{BG}=-10, -5, 0, 5, and 10 V. (c) Dependence of V_{TH} on V_{BG} for TFTs with E_g of 3.1 and 1.1 eV. (d) Transfer curves at V_D=12 V for V_{BG} between -60 V and 60 V for TFTs with E_g of 3.1 and 1.1 eV [6].

Fig. 1 (c) shows the dependence of the calculated V_{TH} on V_{BG} for TFTs with OS E_g of 3.1 and 1.1 eV. Here, 3.1 eV is E_g of a-IGZO and 1.1 eV is that of silicon. When E_g=3.1 eV, V_{TH} changes linearly over the V_{BG} range between -60 and 60 V. In contrast, when E_g=1.1 eV, the range of the linear change is narrowed to between -20 V and 20 V.

Fig. 1 (d) presents simulated transfer curves at V_D=12 V for TFTs with E_g=3.1 and 1.1 eV. For E_g=3.1 eV, the transfer curves shift parallel with respect to the change of V_{BG} in the range between -60 and 60 V. For E_g=1.1 eV, I_D in the subthreshold region is independent of V_{BG} when V_{BG} is below -20 V, and V_{TH} remains constant. Additionally, I_D in the OFF region increases when V_{BG} exceeds 20 V, and V_{TH} cannot be found in this case. The simulations indicate that the characteristics of the TFTs with E_g=1.1 eV are caused by shielding of the electric field from the gate or BG by holes formed by thermal excitation. In contrast, when E_g is 3.1 eV, very few holes are formed via thermal excitation and the electric field from the gate or BG is thus not shielded. As a result, the controllable V_{TH} range of the DG OS TFT is wider than that of the DG Si TFT. The simulations can also reveal that the very low OFF current of the OS TFT originates from the fact that very few holes are formed by thermal excitation or injected from the source/drain electrodes.

3.2 Bilayer-Channel Structure

Stacked-channel OS TFTs contain a stack of OS channel layers with different mobility and stability characteristics, which leads to these devices exhibiting high mobility and stability. Because each channel layer is thin, the OS TFT can turn off even if the stacked channel includes an OS with high mobility and a high carrier-electron concentration (e.g., an OS with a high indium content). Stacked-channel OS TFTs are suitable for investigating the mechanisms of NBTS instability.

NBTS causes negative shifts of the transfer curves and field-effect mobilities of OS TFTs; this degradation depends on the chemical composition of the OS channel [7]. For example, amorphous In-Sn-Zn-O (a-ITZO) TFTs with high mobility of over 30 $cm^2/(Vs)$ show low NBTS stability, whereas amorphous In-Ga-O (a-IGO) with relatively lower mobility of around 20 $cm^2/(Vs)$ exhibit higher NBTS stability. It is supposed that the negative shift is caused by a charge trapping at the interface between the gate insulator and OS channel or a carrier doping in the channel.

Fig. 2 (a) shows the structure of a bilayer channel OS TFT with a stacked channel composed of a 20 nm-thick a-ITZO layer and a 15 nm-thick a-IGO layer. Fig. 2 (b) displays measured field-effect mobilities under an NBTS with V_G of V_{TH} - 20 V. The NBTS causes negative shifts of the mobility at V_G≤10 V. As the NBTS time increases, the voltage where the mobility starts to rise moves to the negative direction and the peak mobility rises. In contrast, there is no change in the mobility at V_G≥10 V.

Fig. 2 (c) shows calculated field-effect mobilities of the bilayer TFT, a-ITZO single-layer TFT, and a-IGO single-layer TFT. The field-effect mobility of the bilayer TFT is comparable with the measured mobility in Fig. 2 (b) and originates from a-ITZO at low V_G and a-IGO at high V_G. This behavior can be explained by considering the energy band diagram of the bilayer channel shown in the inset of Fig. 2 (c). Because the bottom of the conduction band E_C of a-IGO is higher than that of a-ITZO, electrons accumulate within a-ITZO near the interface between a-IGO and a-ITZO at low V_G. The bilayer TFT mobility is

therefore determined by the mobility of a-ITZO. When V_G increases, electrons overcome the barrier, which is lowered by band bending via electric field from the gate, and accumulate within the a-IGO layer near its interface with the gate insulator. In this region, the mobility is mainly dominated by the mobility of a-IGO.

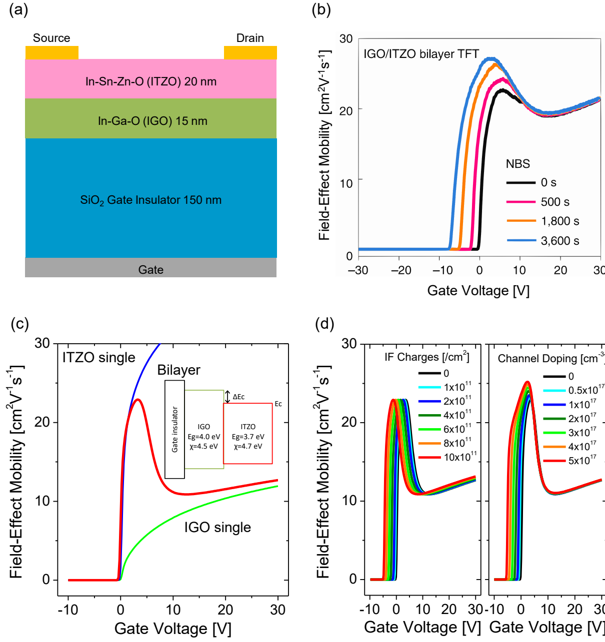

Fig. 2 (a) Structure of a bilayer TFT. (b) Measured field-effect mobilities of the bilayer TFT under NBTS. (c) Calculated field-effect mobilities of bilayer and single-layer TFTs. Inset is the energy band diagram of the bilayer TFT. (d) Calculated field-effect mobilities of bilayer TFTs with various gate interface fixed charge values (left) and a-ITZO carrier doping values (right) [7].

Next, we consider the mechanism of the negative shift of mobility curve under NBTS using the device simulation results. The left of Fig. 2 (d) shows the field-effect mobilities of the bilayer TFT with fixed charges of 0, 1×10^{11}, 2×10^{11}, 4×10^{11}, 6×10^{11}, 8×10^{11}, and 10×10^{11} /(cm^2) at the interface between the gate insulator and a-IGO. Each mobility curve shifts to the negative direction with the shift reflecting the magnitude of the charge increases. Because the shift is the parallel shift of whole mobility curve, it is difficult to describe the measured mobility under NBTS based on interface charge. The right of Fig. 2 (d) shows the field-effect mobilities of the bilayer TFT with carrier doping of a-ITZO of 0, 0.5×10^{17}, 1×10^{17}, 2×10^{17}, 3×10^{17}, 4×10^{17}, and 5×10^{17} /(cm^3). Carrier doping causes a negative shift of only a part of the mobility curve ($V_G \leq 10$ V), and both the mobility peak and shift increase with rising doping density. The calculated mobilities with carrier doping agree well with measured ones under the NBTS in Fig. 2 (b). These results indicate that the negative shift under NBTS is caused by carrier doping.

3.3 Positive Bias Temperature Stress

PBTS causes the transfer curve of the OS TFT to translate in the horizontal direction and causes positive shifts in V_{TH}. The shift with respect to the stress time can be expressed by a stretched exponential function. In general, electron capture processes at the interface traps between the channel and gate insulator are considered to cause a parallel V_{TH} shift. Because the electron capture rate in a Shockley-Read-Hall (SRH) model that represents a general model of the electron capture behavior is given by an exponential function with respect to time, it is difficult to describe the V_{TH} shift using this model.

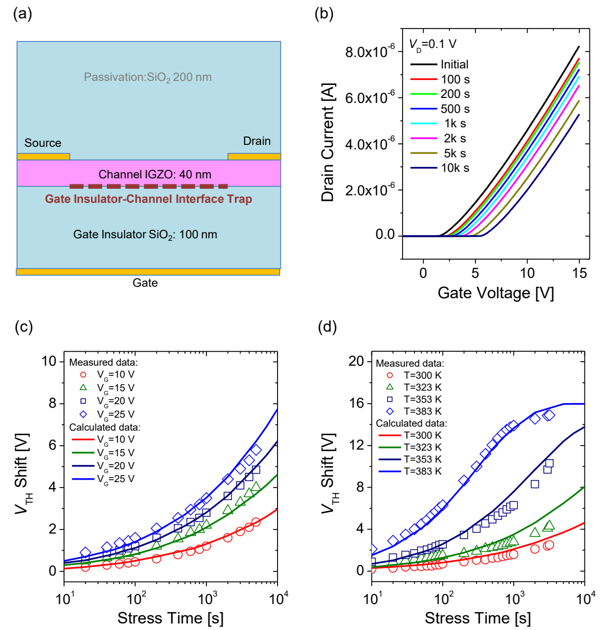

Fig. 3 (a) Structure of the simulated a-IGZO TFT. (b) Calculated transfer curves at V_D=0.1 V under PBTS with T=300 K and stress V_G=15 V. Measured and calculated V_{TH} shifts under PBTS with (c) stress V_G=10, 15, 20, and 25 V at T=300 K, and (d) stress V_G=15 V at T=300, 323, 353, and 383 K [8].

Here we propose an empirical model for the electron capture behavior of the interface traps with an interface electric field dependence [8] to reproduce the observed V_{TH} shift. This model includes a neutral trap state S1 and a negatively charged trap state S2. The transfer rate from S1 to S2 with a electron capture process can be expressed by

$$\frac{dN_{S2}}{dt} \sim C\, e^{-\frac{E_a}{k_B T}} \left[\ln\left(\frac{|\overrightarrow{F_{S0}}|}{|\overrightarrow{F_S}|}\right)\right]^{\beta-1/\beta} N_{S1} \qquad (2)$$

where N_{S1} is the S1 density, N_{S2} is the S2 density, $\overrightarrow{F_s}$ is the interface electric-field, $\overrightarrow{F_{s0}}$ is the initial interface electric-field, E_a is the activation energy, k_B is the Boltzmann constant, T is the absolute temperature, C is the constant model parameter, and β is the power factor that characterizes the stretched exponential function. β is given by

$$\beta = \frac{T}{T_0} - \beta_0 \quad (3)$$

where T_0 is the intrinsic temperature of β and β_0 is the intercept of β.

Figs. 3 (a) and (b) show the structure of the OS TFT used in the simulation and the simulated transfer curves under PBTS when the temperature is 300 K and the stress V_G is 15 V, respectively. Fig. 3 (c) compares the measured and calculated V_{TH} shifts under PBTS conditions when the temperature is 300 K and stress V_G is 10, 15, 20 and 25 V. Fig. 3 (d) shows the measured and calculated V_{TH} shifts under PBTS conditions at temperatures of 300, 323, 353, and 383 K and stress V_G of 15 V. The calculated V_{TH} shifts are close to the measured values. This model reproduces the PBTS degradation of the OS TFT over wide ranges of both temperature and stress V_G. Furthermore, we expect that it may be possible for the model to describe the device degradation under not only PBTS, but also high V_D stress because the model includes the effects of the electric field.

4 Conclusions

In this work, we considered the operation of OS TFTs with a DG structure and a bilayer-channel structure under NBTS. Because the wide E_g of the OS suppresses hole formation via thermal excitation, the DG OS TFT exhibits a wide V_{TH} control range based on V_{BG} and a very low OFF current. Carrier doping of the high mobility OS layer reproduced the behavior of the field-effect mobilities of the bilayer TFT under NBTS. This result indicates that the NBTS-induced negative shift of the mobilities of OS TFTs originates from carrier doping. In addition, we proposed a model that describes the V_{TH} shift of the OS TFT under PBTS. This model includes the effects of the interface electric fields. Device simulations using this model reproduced measured V_{TH} shifts.

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