Recent Progress in Design Automation of Superconductor Circuits

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Abstract

The development of superconducting electronic design automation (S-EDA) is accelerating as technologies and logic families – such as Rapid Single Flux Quantum (RSFQ), Adiabatic Quantum-Flux-Parametron (AQFP), and related variants - continue to mature. In contrast to the long-established CMOS EDA ecosystem, S-EDA has previously relied on custom flows and the interoperability between tools was limited. We present the current state of S-EDA across commercial and open-source offerings, and highlight the practical integration achieved during (and since) the IARPA SuperTools program, particularly through the ColdFlux project [1][2]. SuperTools set ambitious goals for scalable superconducting circuit design, such as ≥10 million Josephson junctions or ≥1 million logic gates, with clock frequencies of at least 100 GHz. These goals required the formation of interoperable design, analysis, and verification tools to ensure success.

Spanning approximately five and a half years, the ColdFlux project brought together global academic contributors to develop open-source and commercial S-EDA capabilities. ColdFlux yielded a powerful suite of tools capable of handling complex digital circuits ranging from device and behavioural modelling to full physical-design and verification [1].

These tools include InductEx [3] and JoSIM [4]. InductEx has undergone continuous development since the ColdFlux project and currently provides three-dimensional parameter extraction and layout verification, along with capabilities ranging from multi-terminal inductance and capacitance extraction to characteristic impedance, S-parameters, magnetic and gradient field analysis, flux-trapping analysis, packaging evaluation, and support for materials with magnetic permeability. Complementing extraction and verification, JoSIM delivers SPICE-syntax circuit simulation with native support for Josephson-junction devices. JoSIM employs modified nodal methods for both voltage and phase, and uses modern sparse solvers to accelerate transient analysis while preserving accuracy in phase-based dynamics. This enables rapid exploration of SFQ timing, bias margins, and clock network behavior, as well as making JoSIM the only simulation engine other than PSCAN [5][6] that can correctly model the coupling from trapped fluxons to circuit elements. The availability of both an open-source implementation and the performance-tuned commercial version JoSIM-Pro helps to bridge the gap between academic prototyping and production-oriented flows.

Recently, the rapid growth of research and development efforts for superconducting qubit systems has placed demands on S-EDA tools for more efficient verification of very large layouts with extremely

small qubit devices, more fidelity for weak coupling calculation between couplers and qubits, efficient frequency characterization for high-Q resonators and tunable couplers, and support for new fabrication layer stacks and junction definitions. The development direction of tools such as InductEx, TetraHenry [7][8] and JoSIM now follow the requirements of superconducting qubit designers, with the near-term goal of automating the entire design and verification process from device layout to the calculation of the Hamiltonian.

The advances achieved throughout the past few years show that S-EDA is transitioning from a niche, fragmented set of tools into a mature and interoperable ecosystem capable of supporting intricate qubit ecosystems and complex and large-scale superconducting circuit design. Integrating specialized tools into cohesive, end-to-end design flows enhances both productivity and verification accuracy, while creating a flexible framework ready to accommodate emerging technologies. This capability is increasingly important as superconducting digital logic, cryogenic systems, and quantum hardware becomes more closely interconnected. As design requirements expand toward ultra-high-speed computing and quantum-integrated systems, continued refinement of these tools - paired with standardized workflows - will be essential to realizing the next generation of large-scale, high-frequency superconducting electronics.

References

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