Demonstration of A Small-Area Unary Arithmetic Logic Unit using Single Flux Quantum Circuits

Zeyu Han[1,*], Nobuyuki Yoshikawa[1,2,3], and Yuki Yamanashi[1,2,3]

[1] *Department of Electrical and Computer Engineering, Yokohama National University, 79-5 Tokiwadai, Hodogaya, Yokohama 240-8501, Japan*

[2] *Institute of Advanced Sciences, Yokohama National University, 79-5 Tokiwadai, Hodogaya, Yokohama 240-8501, Japan* [3] *Institute for Multidisciplinary Sciences, Yokohama National University, 79-5 Tokiwadai, Hodogaya, Yokohama 240-8501, Japan*

Abstract

The Single-Flux-Quantum (SFQ) circuit has emerged as a promising technology for integrated systems, offering high-speed operation and low power consumption. However, the area limitations of current superconducting circuit fabrication technologies pose significant challenges for constructing large-scale SFQ systems. To tackle this challenge, various unconventional computing paradigms have been explored to implement complex operations using simple logic gate circuits. One such approach is unary computing (UC) [1], which represents values by the count of "1"s and clusters all "1"s at the head of a bit sequence. In this work, we design a novel small-area UC-based arithmetic logic unit (ALU) for SFQ circuits. Our ALU implements addition, subtraction, maximum, minimum, and logic operations using only a few logic gates and three NDROs. The test circuits for the proposed ALU, consisting of 1598 Josephson junctions, were fabricated using the AIST HSTP with a critical current density of 10 kA/cm^2 and experimentally verified to operate correctly at frequencies above 60 GHz. Compared to a bit-serial ALU [2], our design reduces the count of logic gates by approximately 55% and achieves a 96% area reduction relative to a 4-bit bit-slice ALU [3]. These results demonstrate that UC-based ALU can realize ultrafast computation with small hardware overhead for energy-efficient superconducting processors.

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