Toward Stable Operation of Si Quantum Computers: Origin of Long-period Charge Fluctuations in Si Fin-type Quantum Dots

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1. Introduction

Si quantum computers (QCs) have attracted considerable attention due to their scalability potential to achieve the large-scale integration of Si spin qubits using CMOS manufacturing technology. Recently, there has been several progresses in the performance of Si spin qubits, such as two-qubit gates operation with fidelity over 99%[1] and prolonged coherence time T_2^* of 120 μsec [2]. From the standpoint of practical use, the electrical stability of qubits is a critical issue that needs to be addressed, as they necessitate frequent monitoring and calibrations of the qubit parameters (Fig. 1). Indeed, some superconducting QCs already in commercial use are calibrated every few hours, preventing the stable operation and limiting the available time slot. However, the electrical stability of Si spin qubits, i.e., long-period charge fluctuation, has not been thoroughly discussed until now. In this study, we conducted an in-depth analysis of the electrical stability of the fin-type Si quantum dots (QDs), which is a promising host for spin qubits. We performed gate-bias-dependent random telegraph noise (RTN) measurements to clarify the physical origin of the long-period charge fluctuation of fin-type QDs for the first time.

2. Experimental Procedure

Fin-type QDs were fabricated on p-type SOI wafers (T_{SOI}=60 nm, T_{BOX}=145 nm) with a 12-nm-thick SiO_2/poly-Si gate (Fig. 2). A plunger gate (PG), barrier gates (BGs), and accumulation gates (AGs) were formed on the fin to confine electrons under the PG. The measurements were performed at 4 K using a cryogenic prober. We confirmed successful single-electron transport at 4 K with fabricated fin-type QDs from the charge stability diagram shown in Fig. 3(a). Figure 3(b) shows the drain current (I_D) transient at a fixed gate bias. A distinct two-level transition was observed with an ultralow frequency of < 0.05 Hz, which would become a critical issue for the stable operation of Si QCs. As the QDs have multiple gates and different bias conditions are used for single-electron transport, it is very difficult to identify the origin of charge fluctuation by the QD measurement alone. Thus, we fabricated the single-gate test device having the same fin and gate structure as QDs, enabling the gate-bias-dependent RTN analysis to reveal the trap states inducing the long-period charge fluctuations (Fig. 4).

3. Results and Discussion

Figure 5(a) shows the I_D-V_G characteristic of a single-gate test device at 4 K. Captured I_D transients at different gate bias conditions from off-state to on-state bias are shown in Figs. 5(b) to 5(g). A distinct multi-level transition was observed at bias conditions of 300, 320, and 340 mV. These are close to V_{th} of 320 mV, and we confirmed the long-period charge fluctuation occurred only at certain bias conditions. We extracted the power spectral density (S_{ID}) from the Fourier transform of the I_D transient (Fig. 6). The S_{ID} showed drain current dependence and increased by more than one order of magnitude toward V_{th}. As the S_{ID} is proportional to the effective trap density (N_{eff}) in the carrier number fluctuation (CNF) model [3], the obtained results indicate that N_{eff} is increased near V_{th}. From the fitting of the S_{ID} -I_D plot based on the CNF model, we extracted the energetic distribution of trap states inducing excess noise near V_{th}. We found the exponentially distributed trap states with shallow decay energy of 20 meV at the conduction band edge are responsible for the charge fluctuation observed near V_{th} (Fig. 7). To reveal where long-period charge fluctuation occurs in fin-type QDs, we performed a simulation of single-electron transport by using an in-house TCAD simulator [4]. Figure 8 shows the simulated Fermi level (E_F) position along the fin-width (A-B) and fin-depth (A-C) directions. We found the E_F aligns to the band edge states in the whole area of the top-surface of the fin, while that of the side-surface is mostly far from the band edge states. This means the long-period charge fluctuations mainly occur at the top-surface of the fin rather than its side-surface. Since the band edge states are strongly related to the quality of the MOS interface [5], these results imply that the MOS interface engineering at the top-surface of the fin is critical to improve the electrical stability of the fin-type QDs.

4. Conclusions

We conducted the first experimental verification on the long-period charge fluctuation of fin-type QDs, whose origin is band edge states located at the top-surface of the fin, suggesting that even more care of the MOS interface at the fin-top is necessary to provide better stability. We believe that the obtained knowledge paves the way to realize stable quantum computation with Si spin qubits.

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References [1] A. R. Mills *et al*., Sci. Adv. **8**, eabn5130 (2022). [2] M. Veldhorst *et al*, Nat. Nanotechnol. **9**, 981 (2014). [3] G. Ghibaudo *et al*., Phys. Stat. Solidi (a) **124**, 571 (1991). [4] H. Asai *et al*., Jpn. J. Appl. Phys. **62**, SC1088 (2023). [5] H. Oka *et al*., Tech. Dig. IEDM, 22-6 (2023).

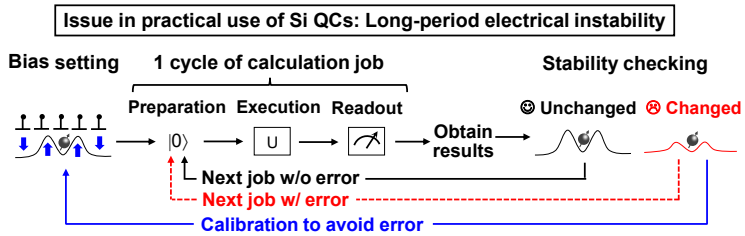

Fig. 1 The aim of this study is to clarify the origin of long-period charge fluctuation of Si QDs that necessitates frequent monitoring and calibration during its running time.

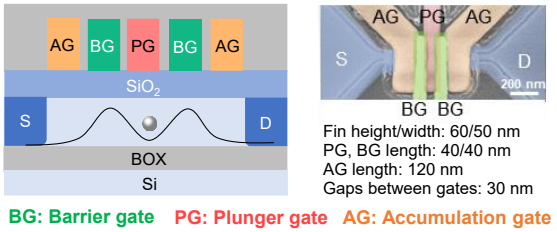

Fig. 2 Fabricated fin-type QDs on SOI wafer. The gate bias condition was chosen to confine an electron using a potential barrier formed by PG, BG, and AG.

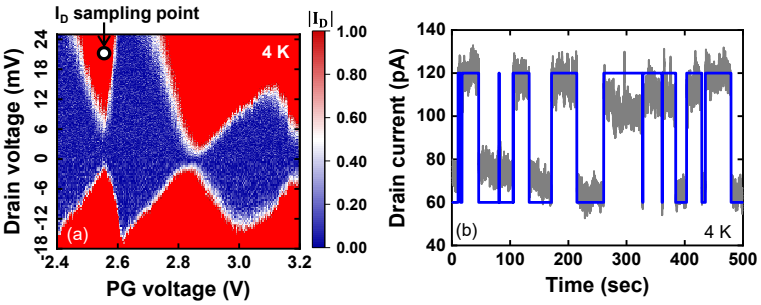

Fig. 3 (a) Charge stability diagram of fin-type QDs. (b) I_D transient of fin-type QDs with gate bias condition indicated in (a).

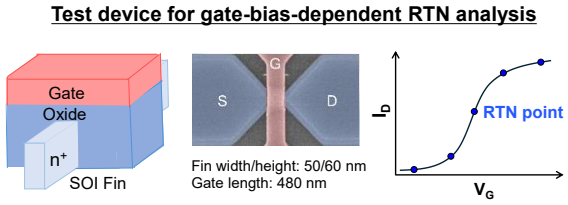

Fig. 4 Single-gate test device, which is fabricated on the same wafer with the same process as the fin-type QDs. Gate-bias-dependent RTN analysis was conducted to clarify the origin of charge fluctuation.

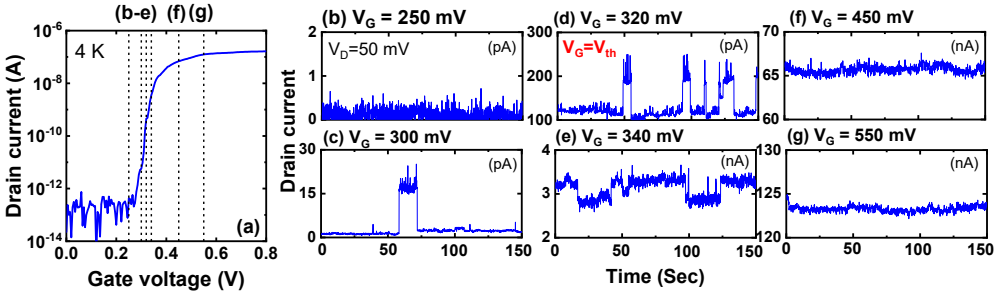

Fig. 5 (a) I_D-V_G curve and transient of I_D of single-gate test device at 4 K with gate bias of (b) 250 mV, (c) 300 mV, (d) 320 mV, (e) 340 mV, (f) 450 mV, and (g) 550 mV. Trapping/de-trapping events observed only near the V_{th} operation.

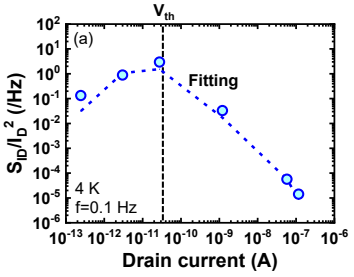

Fig. 6 I_D dependence of S_{ID}/I_D^2. Excess noise appeared near V_{th}. The fitting curve is also shown.

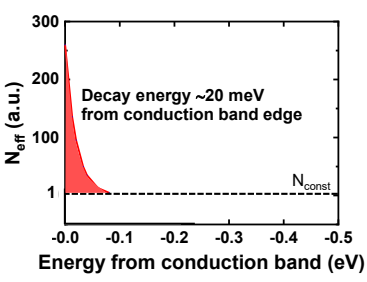

Fig. 7 Extracted energetic distribution of trap states from fitting of S_{ID} shown in Fig. 6.

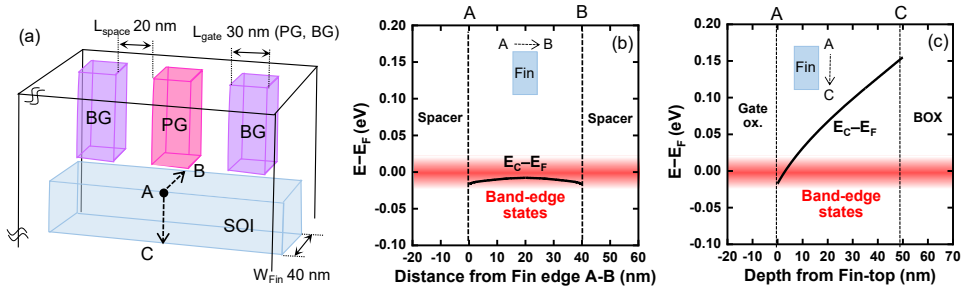

Fig. 8 (a) Structure of simulated fin-type QDs. Simulated energy level of E_C relative to E_F (E_C–E_F) along with (b) fin width A-B and (c) fin depth A-C. Position for conduction band edge operation (E_F–E_C <20 meV) is marked by red areas.