Advanced Logic Transistor Innovation Towards "Beyond 2nm" Technology

Toshiro Hiramoto[1,3] and Hitoshi Wakabayashi[2,3]
[1]The University of Tokyo, [2]Institute of Science Tokyo, [3]LSTC
Email: hiramoto@nano.iis.u-tokyo.ac.jp

1. Introduction

The rapid global advancement of AI is fundamentally supported by progress in semiconductor technology, particularly in advanced logic devices. As AI applications continue to expand, the demand for computing power has been growing exponentially, driving an urgent need for further innovation in semiconductor scaling and performance. Recognizing the strategic importance of semiconductors in the AI era, governments around the world have announced major investments in their domestic semiconductor industries. Japan has also launched a national initiative to strengthen its semiconductor capabilities. In 2022, Rapidus Corporation was established with the goal of mass-producing 2nm logic chips, and the Leading-edge Semiconductor Technology Center (LSTC) [1] was also founded to conduct research and development on “beyond 2nm” technologies. In this presentation, recent trends in logic semiconductor devices are reviewed, and the ongoing R&D activities at LSTC are introduced.

2. Histrical and Future Trend

Figure 1(a) [2] shows the historical and future trend of semiconductor logic technology nodes since 1980, plotted based on data from major international conferences and the IRDS roadmap [3]. It is remarkable that the nominal technology node has continued to shrink for more than 45 years, following an almost exponential pace of miniaturization. In 2024, TSMC presented its 2nm logic technology [4], and in 2025, Intel announced its 18A technology [5]. However, despite continued scaling, the rate of improvement in device speed and energy consumption has slowed compared with the past, mainly due to fundamental physical limitations and increasing parasitic effects, as illustrated in Figure 1(b). Moreover, the rise in chip power density, shown in Figure 1(c) [2], has become a critical concern, posing serious challenges for overall system performance and energy consumption.

3. Project for “Beyond 2nm”

To address these challenges, LSTC is conducting the NEDO project titled “Technology Development for Beyond 2nm and Short TAT Semiconductor Manufacturing.” In this project, elemental process technologies for “beyond 2nm” devices with scalability toward the 1nm node and beyond are being developed, as summarized in Table 1. The main research topics include: Gate stack technology, aiming at CET scaling and Vth control, BEOL technology focusing on the development and reliability of new interconnect materials, and epitaxial growth technology for (110) substrates to enhance channel mobility and device performance.

4. Summary

LSTC was established for the development of “beyond 2nm” technologies. Main topics are the gate stack technology, BEOL, and the epitaxial growth technology.

References

[1] https://www.lstc.jp/.
[2] Data has been updated based on T. Hiramoto and H. Wakabayashi, IEEE Silicon Nanoelectronics Workshop, 2024.
[3] International Roadmap for Devices and Systems (IRDS), More Moore, 2024 Edision, https://irds.ieee.org/.
[4] H. C. Lin et al., IEDM, 2024.
[5] K. Fischer et al., VLSI, 2025.

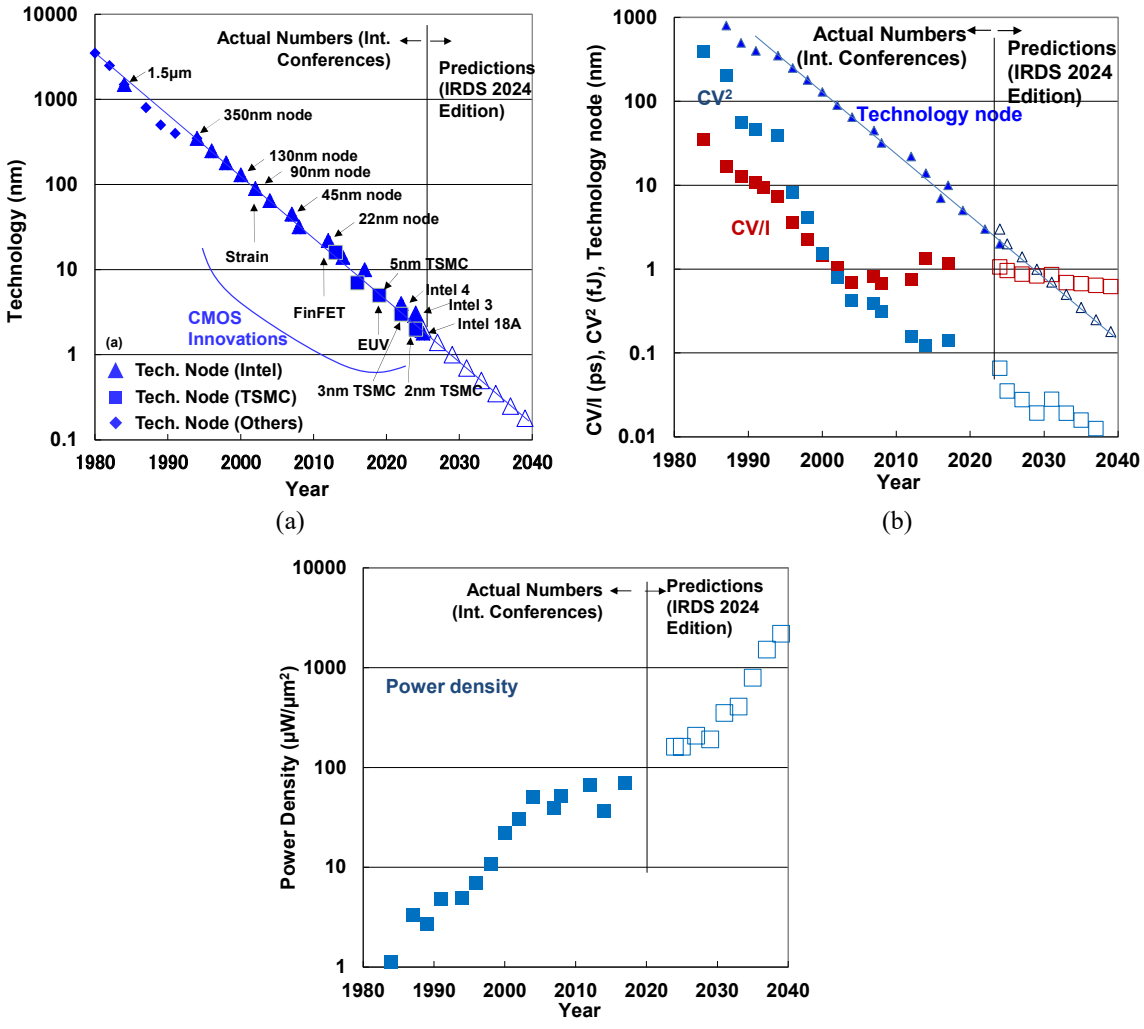

Fig. 1. (a) Hisetrical and future trend of the technology node. (b) Trends of device delay time (CV/I) and energy (CV^2). (c) Trend of power density.

Table 1. Development items in “Technology Development for Beyond 2nm and Short TAT Semiconductor Manufacturing” in LSTC.

Items	Development focus
(1) Gate Stack	CET scaling, Vth control by dipoles and WF, Reliability.
(2) BEOL	New interconnect materials by MI, Reliability and Characterization of Post Cu interconnect.
(3) Epitaxial Growth	(110) substrate and epitaxial growth, Nanosheet formation, S/D epitaxial growth, Contact resistance.