Device Design Trade-off in Silicon Junctionless Floating-Body FeFET

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1. Introduction

Ferroelectric field-effect transistor (FeFET) has been drawing attention in recent decades since the discovery of HfO_2-based ferroelectric materials, mainly due to its CMOS compatibility and potential for high-density memory. While the memory properties of FeFET on bulk substrates have been widely studied [1], an understanding is still limited for FeFET with a thin floating body, which is currently taken into consideration when employed in scaled structures [2] and in 3D ferroelectric NAND [3]. In this work, we study the memory characteristics of floating-body FeFET through the TCAD simulation of junctionless silicon-on-insulator (SOI) FeFET, aiming to gain our understanding of the design trade-off between the memory window and cut-off characteristics.

2. Experimental Procedure

We explored the device characteristics of a junctionless SOI n-type FeFET with 10-nm $HfZrO_2$ (HZO) by TCAD simulation. The structure of investigated device is presented in Figure 1, with an 1-nm interfacial SiO_2 layer and gate work function (WF) as 4.6 V. The SOI is of uniform doping profile. The carrier transport was modelled by drift diffusion. The relative permittivity was $\varepsilon_r = 35$ for ferroelectric HZO. The remanent polarization was $P_r = 20$ μC/cm^2 and the coercive field was $E_C = 1.16$ MV/cm, respectively [3].

Quasi-static simulations were performed under a slow bidirectional gate voltage (V_g) sweep for 1000 s. $V_{th,avg}$ is defined as the center V_{th} of the two V_{th} states, where each V_{th} is defined by the constant current level of $W/L\times10^{-7}$ A. Memory window (MW) is defined as MW = $\Delta E_C' \times T_{HZO}$, where $\Delta E_C'$ is the separation of the two effective coercive field in the polarization minor loop.

3. Results and Discussion

Figure 2 plots typical relationships between polarization and electric field under bidirectional sweep of $V_g = \pm15$ V. As there is no hole contact in the junctionless floating-body structure, holes in channel were suppressed, resulting in a lack of positive charges to produce the sufficient electric field and switch polarization in HZO at negative V_g.

Figure 3 shows $V_{th,avg}$ with various combinations of doping concentration N_D and SOI channel thickness T_{SOI}. With higher N_D or thicker SOI, it is more difficult to turn off the channel. This can be seen in the severely negative value of the center threshold voltage. We further discuss the depletion region by depicting electron distribution in Figures 4(a) and 4(b) with different N_D and T_{SOI}. Under same negative gate bias, a device with lower N_D and thinner SOI is easier to fully deplete the channel.

The carrier distribution under different N_D and T_{SOI} leads to different electric field distribution, as shown in Figures 5(a) and 5(b). With higher N_D or thicker SOI in the channel, a large electric field in the ferroelectric layer would be easily produced at the negative gate voltage condition, resulting in a better polarization switching and an improved memory window as shown in Figure 6. Here, the relation with maximum depletion charge $Q_{dep} = qN_DT_{SOI}$ is also indicated in the plot as a common criterion. Whereas low N_D or thinner SOI is favourable to achieve a channel with better cut-off, the opposite is yet favourable to achieve better MW, implying that there exists the proper design space. From our result, it is observed that when Q_{dep} is smaller than 1 μC/cm^2, the MW is limited to as small as 1.1V; on the other hand, when Q_{dep} is larger than 2 μC/cm^2, the $V_{th,avg}$ rapidly shifts away from zero. We concluded that with N_D and T_{SOI} leading to Q_{dep} between 1 and 2 μC/cm^2, e.g., $N_D = 10^{19}$ cm^{-3} and $T_{SOI} = 10$ nm, both improved MW and reasonable cut-off can be obtained.

4. Conclusions

By TCAD simulation, we studied the memory window and threshold voltage in junctionless floating-body FeFET device. We described the impact of doping concentration and channel thickness on the cut-off behavior and the memory property and discussed the design space of such FeFET.

Acknowledgements

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References

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[2] W. Huang et al., IEEE Electron Device Lett. **43**, 25 (2022).
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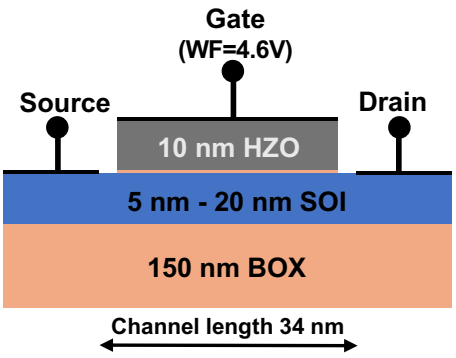

Fig. 1 Device structure of SOI FeFET.

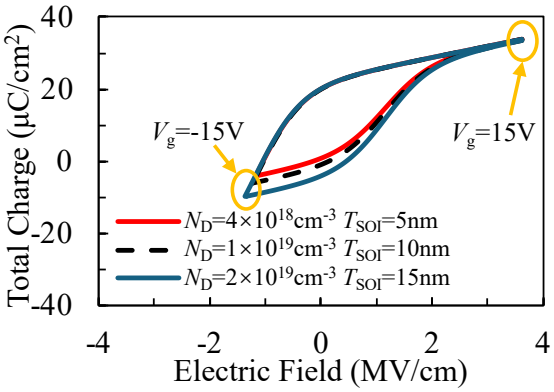

Fig. 2 Polarization loop in proposed device.

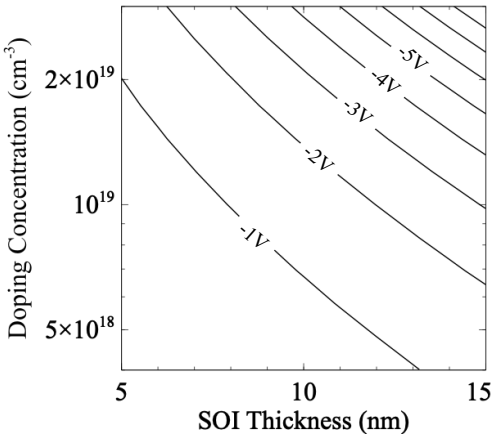

Fig. 3 Center threshold voltage $V_{th,avg}$ in relation to N_D and SOI thickness.

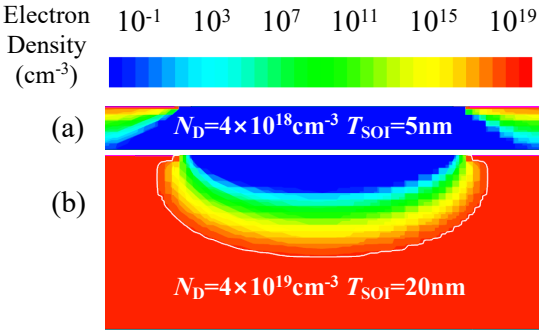

Fig. 4 Electron distribution in the SOI channels of (a) T_{SOI}=5 nm and N_D=4×10^{18} cm^{-3} and (b) T_{SOI}=20 nm and N_D=4×10^{19} cm^{-3} under V_g=-10V, respectively. The depletion region edge is drawn with white solid line.

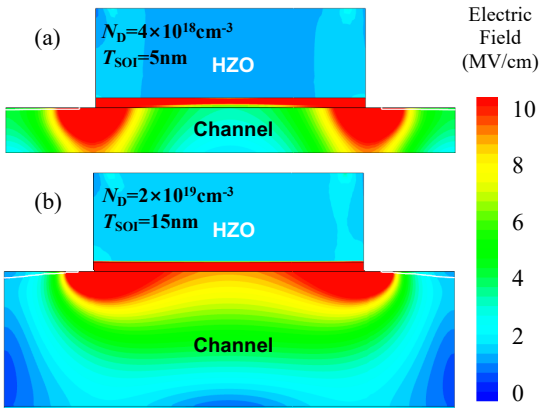

Fig. 5 Electric field distribution in the devices of (a) T_{SOI}=5 nm and N_D=4×10^{18} cm^{-3} and (b) T_{SOI}=15 nm and N_D=4×10^{19} cm^{-3} under V_g=-15V, respectively.

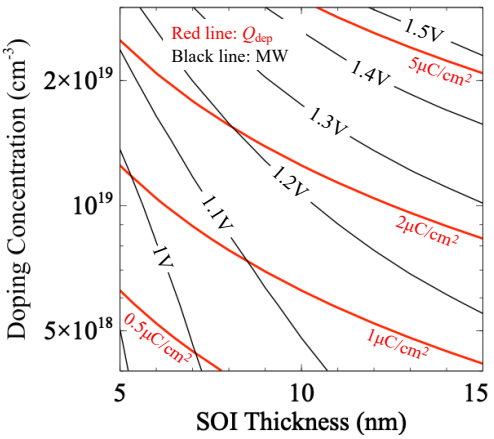

Fig. 6 Memory window MW (black line) and maximum induced charge Q_{dep} (red line) in relation to N_D and SOI thickness.