Electrical Characteristics of 3D CMOS Formed with SiGe pFinFET and IGZO nTFT

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1. Introduction

The monolithic 3D integrated circuits (M3D-ICs) technology is promising to overcome area constraints and move toward more-than-Moore's law [1]. Instead of the single-crystalline silicon, high mobility silicon-germanium (SiGe) channel material was utilized in the coming sub-5 nm logic circuit architectures [2]. However, the performance of p-channel SiGe devices is significantly superior to that of n-channel SiGe devices. This performance mismatch limits the performance of CMOS inverters. On the other hand, n-channel amorphous oxide materials (AOS) have attracted significant attention in recent years due to their advantages such as high mobility, low leakage current, substrate independence, low cost film formation, and high production yield. Among them, a n-channel indium gallium zinc oxide (IGZO) has even been used in M3D-ICs application for its low thermal budget fabrication process, which is compatible with the BEOL temperature limitation and avoids the degradation of FEOL devices. Correspondingly, there is currently no suitable p-channel AOS material that can effectively complement n-channel AOS materials. In this work, a vertically-stacked logic circuit architecture based on a bottom p-channel SiGe FinFET and top n-channel IGZO TFT is demonstrated to reduce the footprint of devices and increase the chip density. It may provide a promising potential for the high performance hybrid integration circuit.

2. Experimental Procedure

The bottom SiGe pFinFETs were fabricated on diced 8-inch SOI wafers, while SiGe epitaxial layer was implanted with P^{31+} ions at 25 keV with a dose of 1×10^{13} cm² and followed with an annealing process at 500 °C for 90 s. Then, a 5 nm thick HfO_2 gate dielectric layer was deposited by ALD and a 100 nm thick TiN metal gate was deposited by sputtering. After fin formation by SADP lithography and ICP-RIE etching, p-channel source/drain regions were implanted with B^{11+} ions (15 keV, 1×10^{15} cm^{-2}), followed by activation at 500 °C for 90 s. Afterwards, a 100 nm thick SiO_2 was formed as isolation layer between bottom and top device, while the interconnect contact holes were opened and a 100 nm thick AlSiCu metallization was filled in by PVD. Then, a 100 nm thick TaN was formed by sputtering as gate electrode for the top IGZG nTFT and patterned by a lift-off process. Then, a 5 nm thick HfO_2 was deposited as gate dielectric by ALD, a 6 nm thick IGZO was deposited as channel layer by sputtering, and a 105 nm thick TaN/Al was formed as source/drain and interconnect electrodes by PVD. A schematic illustration of the monolithic vertical integration with the bottom SiGe pFinFET and top IGZO nTFT is shown in **Fig. 1**.

3. Results and Discussion

Fig. 2 shows the cross-sectional TEM image of CMOS inverter with M3D-ICs structure. It is clear that the bottom SiGe pFinFET and top IGZO nTFT have been successfully vertically integrated. **Fig. 3** shows the I_{DS}-V_{GS} of the (a) bottom SiGe pFinFET and (b) top IGZO nTFT, and the I_{DS}-V_{DS} of (c) bottom SiGe pFinFET and (d) top IGZO nTFT, respectively. The bottom SiGe pFinFET shows a I_{ON}/I_{OFF} ratio of 7.42 order, a S.S. value of 94.78 mV/dec, a V_{TH} of -211 mV, a I_{ON} of 57.62 μA/μm, and a I_{OFF} of 2.19×10^{-6} μA/μm, while the top IGZO nTFT exhibits a I_{ON}/I_{OFF} ratio of 8.22 order, a S.S. value of 66.34 mV/dec, a V_{TH} of 132 mV, a I_{ON} of 0.7 μA/μm, and a I_{OFF} of 4.21×10^{-9} μA/μm. **Fig. 4** exhibits (a) V_{OUT}-V_{IN} curve and (b) voltage gain for CMOS inverter with M3D-ICs structure. A typical V_{OUT}-V_{IN} transfer curve and a high peak voltage gain of 68 V/V can be achieved for this vertically-stacked CMOS inverter architecture.

4. Conclusions

In this work, a 3D monolithic vertically-stacked CMOS inverter is fabricated with high performance bottom SiGe pFinFET and top IGZO nTFT. The architecture can effectively reduce device footprint and further increase

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the chip density of the M3D-ICs. All the processes are compatible with the BEOL process, which has great potential in next-generation semiconductor technology.

References

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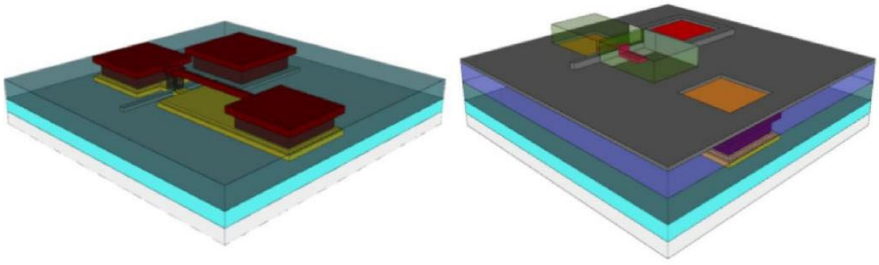

Fig. 1 Schematic illustration of the monolithic vertical integration with the bottom SiGe pFinFET and top IGZO nTFT.

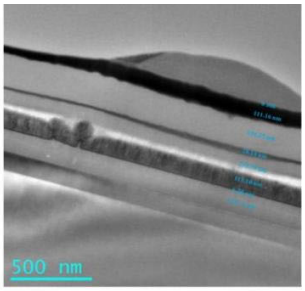

Fig. 2 The cross-sectional TEM image of CMOS inverter with M3D-ICs structure.

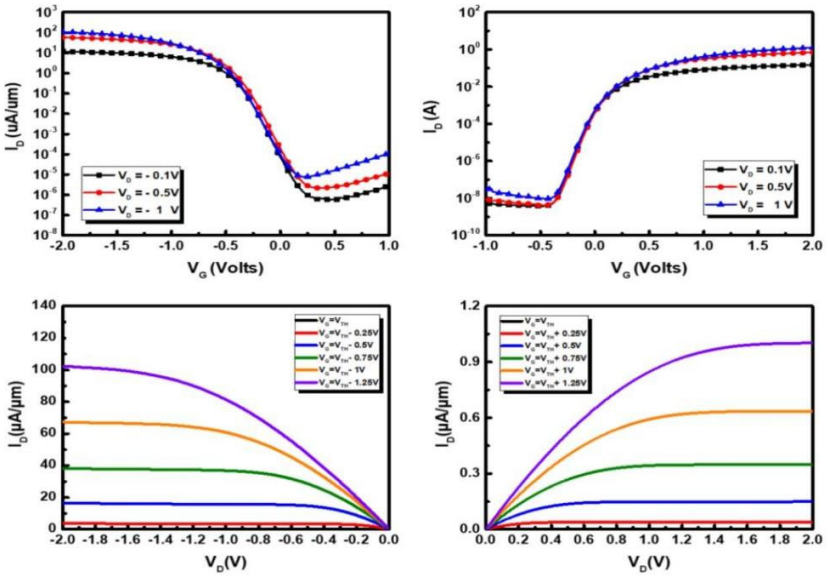

Fig. 3 The I_{DS}-V_{GS} of the (a) bottom SiGe pFinFET and (b) top IGZO nTFT, and the I_{DS}-V_{DS} of (c) bottom SiGe pFinFET and (d) top IGZO nTFT, respectively.

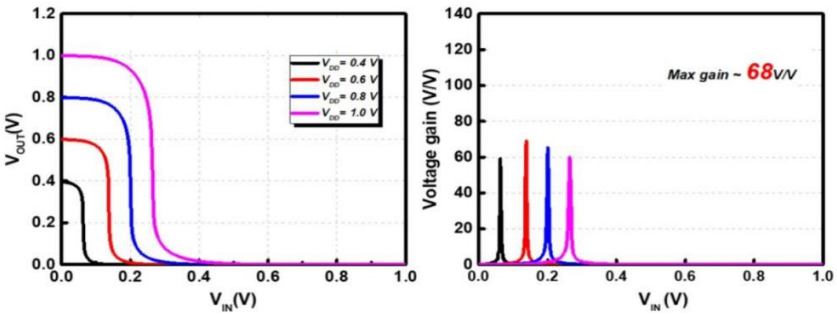

Fig. 4 (a) V_{OUT}-V_{IN} curve and (b) voltage gain for CMOS inverter with M3D-ICs structure.

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