Defect Characterization of 3D Channel-All-Around Transistors Using Variable Photocurrent Method

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1. Introduction

Scaling of DRAM requires transistors with extremely low off-state leakage and high drive current, driving the adoption of three-dimensional (3D) architectures, such as channel-all-around (CAA) transistors [1]. In_2O_3-based oxide semiconductors are attractive channel materials due to their extremely low off-state current, multilayer stacking capability, and highly conformal ALD growth for high-aspect-ratio structures. However, channel defects can impact 3D device performance, and conventional characterization techniques face limitations in such geometries (**Table 1**) [2–4]. For example, uv-vis can only probe defects in thick films, photoluminescence (PL) is challenging for 3D channel spectroscopy, and C-V measurements are complicated by defect coupling. This work applies the Variable Photocurrent Method (VPM) [5] to probe defect states in CAA transistors as a representative 3D architecture.

2. Experimental Procedure

The schematic of the VPM testing system consists of a light-emitting module, a monitoring and feedback module, and an electrical testing module, as shown in **Fig. 1**. Light of different wavelengths sequentially illuminates the device, exciting electrons from defect states within the In-Ga-O (IGO) bandgap into the conduction band, where they contribute to conduction. This generates a photocurrent that is measured electrically, enabling probing of defect states across the bandgap. The fabrication flow of the representative CAA transistor is summarized in **Fig. 2(a)**, with its schematic in **Fig. 2(b)**. The top view (**Fig. 2(c)**), TEM (**Fig. 2(d)**), and EDS mapping (**Fig. 2(e)-(k)**) of the fabricated CAA transistor confirm the 3D geometry, conformal ALD-grown oxide channel, and elemental distribution of different elements.

3. Results and Discussion

Fig. 3(a) shows the transfer characteristics (IV) of CAA transistors under different annealing conditions. A positive shift in threshold voltage (V_{th}) is observed after rapid thermal annealing (RTA) in N_2. This shift may be attributed to a reduction in oxygen vacancy (V_O) defects, which results in a decreased density of donor-like states in the channel. **Fig. 3(b)** presents the responded photocurrent under illumination with different wavelengths measured by VPM, where the as-deposited device exhibits higher photocurrent than the annealed device. Furthermore, **Fig. 3(c)** shows the absorption coefficient (α) extracted from the photocurrent, reflecting defect states within the bandgap. After annealing, a reduction in α across the bandgap is observed, indicating a decrease in V_O defects, particularly near the valence band. The reduction in donor-like states makes channel conduction more difficult, requiring a more positive gate voltage to turn on the transistor, which explains the observed positive shift in V_{th} in the IV curves.

To investigate possible asymmetry in the 3D CAA device, the transistor is measured under two bias conditions, applying 1V to the top bit line (BL) electrode or the bottom word line (WL) electrode while the other electrode is grounded. As shown in **Fig. 4(a)**, applying 1 V to the BL results in a higher on-state current and a positive shift in V_{th}. The larger on-state current may be attributed to structural asymmetry, where the upper channel possesses a higher effective W/L. The observed threshold voltage shift is likely associated with the distribution of V_O defects. **Fig. 4(b)** presents the VPM-measured photocurrent under the same bias conditions. When 1 V is applied to the BL, the photocurrent is lower, whereas when 1 V is applied to the WL, a higher photocurrent response is observed. **Fig. 4(c)** shows the α extracted from the photocurrent. Applying 1 V to the BL, a lower absorption is observed, suggesting a reduced density of V_O defects near the upper channel. This reduction may be explained by two factors. First, the upper channel is more exposed to atmospheric O_2, which can fill V_O. Second, incomplete etching near the bottom leaves more V_O, with subsequent channel deposition providing additional oxygen. The increased V_O near the bottom channel is reflected as higher absorption. These observations are consistent with the IV curves, where the upper channel, having fewer V_O, exhibits a positive shift in threshold voltage, demonstrating a non-uniform defect distribution along the stacked channel.

4. Conclusions

The applicability of the VPM to 3D CAA transistors has been demonstrated. VPM reveals that annealing effectively passivates V_O defects and verifies the channel asymmetry in stacked devices. These results highlight VPM as an effective tool for characterizing defects in 3D oxide semiconductor devices, providing insights for material and process optimization in future DRAM applications.

Method	Excitation /Detection	In-situ devic characterization	Thickness
VPM	**optical /electrical**	**Yes**	**Thin**
UBPC	optical /electrical	Yes	Thin
C-V	electrical / electrical	Yes	Thin
uv-vis	optical / optical	No	Thick
PL	optical / optical	Yes	Thin

Table 1 Benchmark comparison of VPM and conventional methods. This benchmark highlights the advantages of VPM for in-situ, device-level defect characterization in 3D oxide semiconductor device.

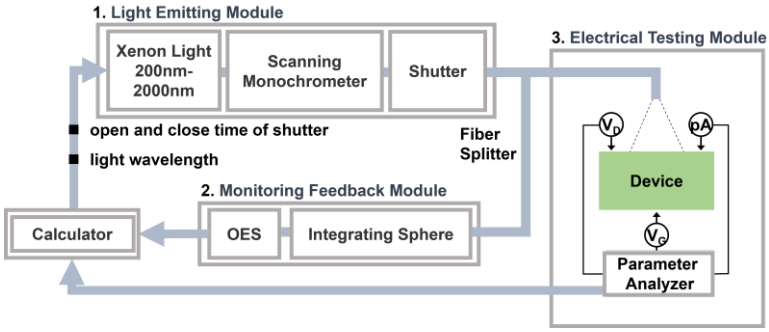
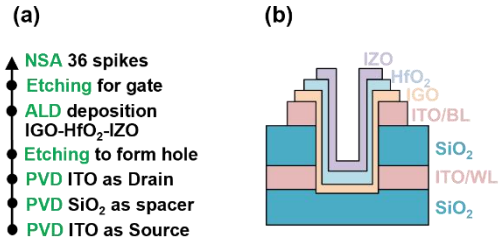


Fig. 1 The schematic of the VPM testing system, comprising a light-emitting module, a monitoring feedback module, and an electrical testing module using a Keithley parameter analyzer 4200-SCS.



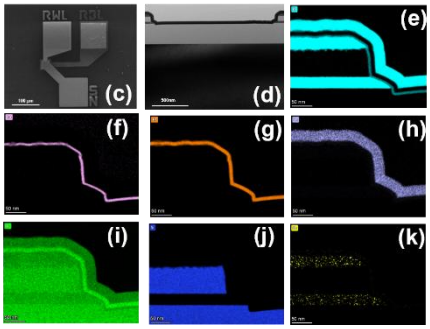


Fig. 2(a) Fabrication flow of the representative CAA transistor; **(b)** device schematic; **(c)** top-view SEM image; **(d)** cross-sectional TEM showing the 3D channel structure; **(e)-(k)** EDS results of In, Ga, Hf, Zn, O, Si, and Sn.

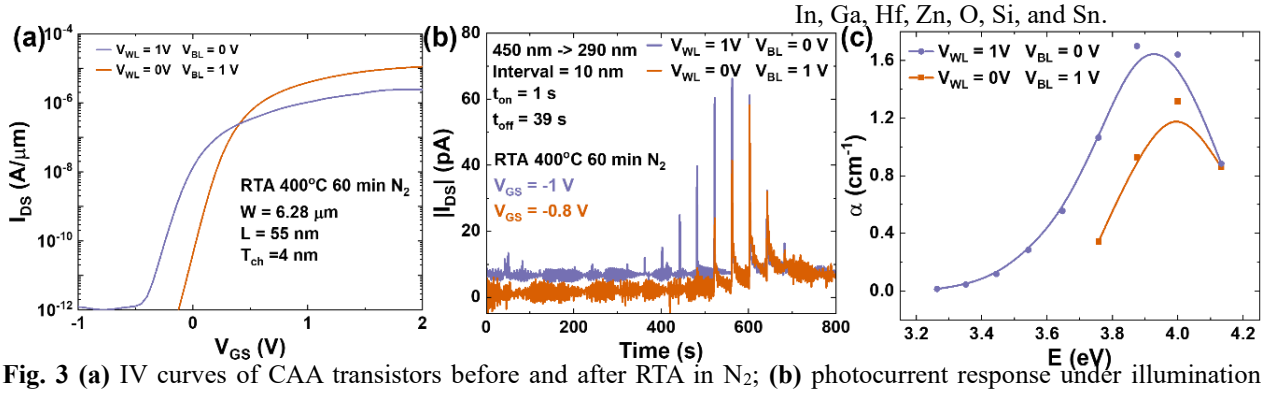


Fig. 3 (a) IV curves of CAA transistors before and after RTA in N_2; **(b)** photocurrent response under illumination at different wavelengths; **(c)** α extracted from the photocurrent, reflecting defect states within the bandgap.

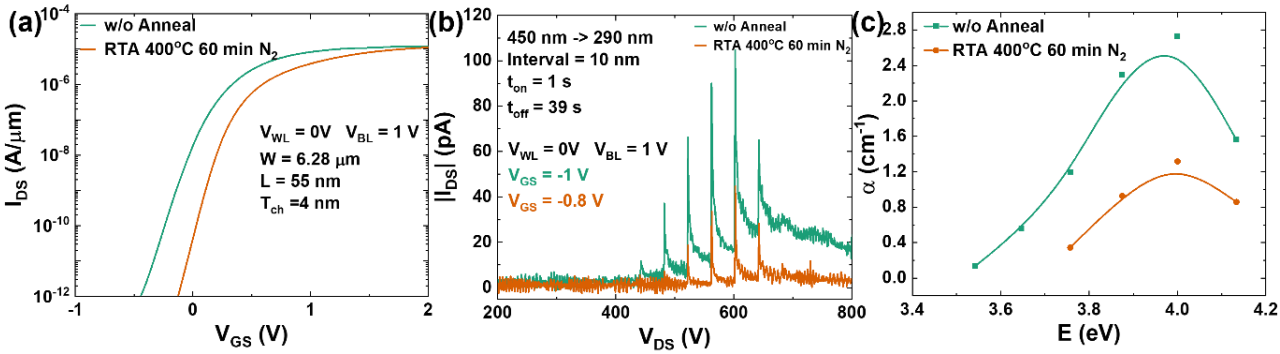


Fig. 4 (a) IV curves of a CAA transistor when 1 V is applied to either the top BL electrode or the bottom WL electrode; **(b)** photocurrent measured by VPM under the same bias conditions; **(c)** α extracted from VPM photocurrent.

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