Unique techniques of ALD for semiconductor devices

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1. Introduction

Atomic layer deposition (ALD) technique is the optimal approach to fabricating conformal films on three-dimensional structures for semiconductor devices such as GaN and Ga_2O_3 power devices, metal/high-k CMOS, oxide-semiconductor FET, DRAM, and FeRAM. ALD sequence generally consist of four steps: (a) Adsorption of precursor gas on the substrate, (b) Ar purge gas to exhaust residual precursor gas into chamber, (c) Reactant gas (H_2O, O_3, O-plasma, NH_3, N-Plasma, etc.) to form target films (oxide, nitride, etc.) on substrate, (d) Ar purge gas to exhaust residual reactant gas into chamber. The four steps constitute one ALD cycle, and the growth rate is expressed as GPC. The GPC which depends on the precursor, ranges 0.03~0.2 nm/cycle. Until now, numerous studies have been conducted using the unique features of ALD. In this paper, I introduce several topics such as dipole control by ALD cycles for metal/high-k CMOS, selective adsorption of TDMAS precursor on HfO_2 underlayer, and GaN surface modification by ALD-dummy-SiO_2 technique, mainly obtained in the author's group.

2. Dipole control by ALD cycle for metal/High-k CMOS

ALD became popular with the HfO_2 film deposition as gate insulator of metal/high-k CMOS in around 2000 year. Metal/high-k CMOS is currently based on the GAA structure as shown in **Fig. 1**. To control V_{th}, the insertion of dipole layer between the HfO_2 and SiO_2 interfacial layer and WFM layer between the HfO_2 and TiN gate electrode is being studied. La_2O_3, Y_2O_3, and Al_2O_3 have been mainly investigated as dipole layers for n- and p-MOSFETs, respectively [1,2]. It has been reported that V_{th} can be easily controlled by each ALD cycle. WFM was also fabricated using the ALD method by doping TiN with elements such as Al and O.

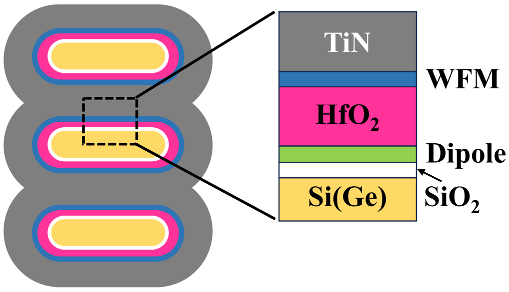

Fig. 1. Schematics of GAA (Gate-All-Around) structure with dipole and WFM layers.

3. Selective adsorption of TDMAS precursor on HfO_2 underlayer

GaN MOS devices with amorphous $HfSiO_x$, $AlSiO_x$ and $HfAlO_x$ gate insulators have been widely investigated as a means of obtaining superior device performance such as high g_m and low leakage current [3,4]. $HfSiO_x$ film was generally formed from the $(HfO_2)_m/(SiO_2)_n$ laminate. Therefore, accurate GPC of the SiO_2 layer deposited via ALD with TDMAS ($SiH(N(CH_3)_2)_3$) precursor on the HfO_2 layer was required. The GPC (0.22 nm/cycle) of ALD-SiO_2 film on HfO_2 underlayer significantly increased compared to that on SiO_2 underlayer (0.043nm/cycle) [5]. To understand this behaviour, we studied the GPC of ALD-SiO_2 on various metal-oxide (M-O) underlayer. Surprisingly, the GPC of the ALD-SiO_2 film increased in the following order: $HfO_2 > TiO_2 > Al_2O_3 > SiO_2 > Ga_2O_3$. Furthermore, we found a correlation between the GPC of the ALD-SiO_2 film and the difference in the electronegativity of the M-O underlayer as shown in **Fig. 2**. Considering to ALD-SiO_2 growth mechanism, the Si atom which has a low positive charge, of the TDMAS precursor is selectively adsorbed toward the O atoms which has a high negative charge, of the M-O underlayer. As a results, a large amount of the TDMAS precursor adsorbed on HfO_2 unerlayer and led to high GPC. Based on these experimental data, we were able to fabricate the targeted Hf/Si ratio in the $(HfO_2)_m/(SiO_2)_n$ laminate.

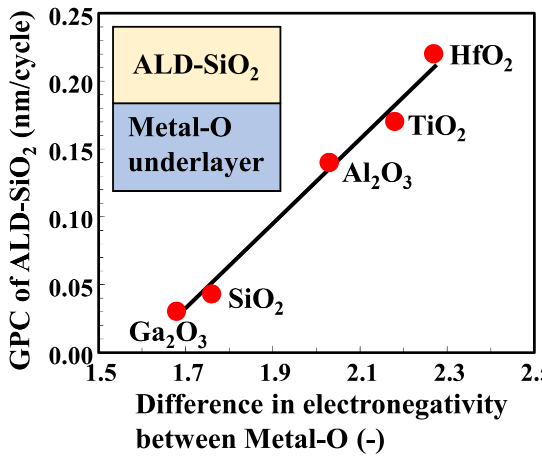

Fig. 2. Correlation between the GPC of the ALD-SiO_2 film and the difference in the electronegativity of M-O.

4. GaN surface modification by ALD-dummy-SiO_2 technique

In GaN MOS capacitors, there is a native oxide (GaO_x) film grown epitaxially on the GaN surface, which act as an electrically unstable GaO_x layer [6]. To modify the unstable GaO_x layer on GaN surface, we proposed ALD-dummy-SiO_2 technique, which is a unique and simple process as shown in **Fig. 3** [7,8]. ALD-dummy-SiO_2 layer (5 nm) was deposited on GaN and subsequently annealed at 800 °C in N_2. The ALD-dummy-SiO_2 layer was removed with BHF solution. Next, a 10-nm-thick Al_2O_3 insulator was deposited on the modified GaN substrate via ALD at 300 °C. Finally, Pt gate electrode and Ti/Pt ohmic contact were formed to fabricate n-GaN/Al_2O_3/Pt capacitor (ALD-dummy-SiO_2). A n-GaN/Al_2O_3/Pt capacitor was also prepared without the ALD-dummy-SiO_2 process as reference (Standard). **Figure 4** shows the V_{fb} shift as a function of bias V-V_{fb} of the ALD-dummy-SiO_2 and Standard capacitors under positive bias stress. The V_{fb} shift of the ALD-dummy-SiO_2 significantly reduced compared to that of the Standard. This is because the unstable GaO_x layer was removed and oxygen-ordered GaO_x layer was formed on the surface of GaN [9]. As a result, the modified GaN led to superior characteristics such as a small V_{fb} shift under PBS.

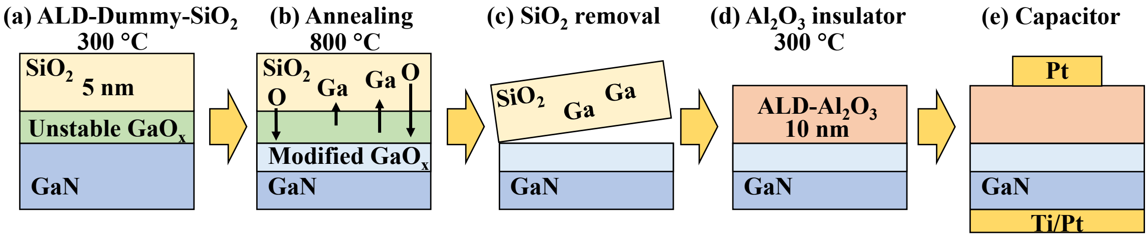

Fig. 3. Schematics of GaN surface modification and capacitor fabrication by ALD-dummy-SiO_2 technique.

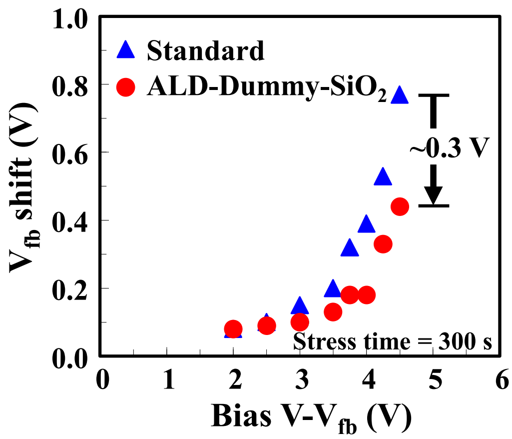

Fig. 4. The V_{fb} shift as a function of bias V-V_{fb} of the ALD-dummy-SiO_2 and Standard capacitors under PBS.

I concluded that ALD is not the use as the equipment, but rather the utilization of its unique characteristics.

Acknowledgements

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References

[1] K. Iwamoto et al., Appl. Phys. Lett. **92**, 132907 (2008).
[2] H. Arimura et al., Abst. of VLSI2025, T19-3 (2025).
[3] K. Ito et al., J. Appl. Phys. **129**, 084502 (2021).
[4] T. Nabatame et al., Appl. Phys. Express **12**, 011009 (2019).
[5] E. Maeda et al., Jpn. J. Vac. Sci. Technol. A **38**, 02409 (2020).
[6] K. Yuge et al., Semicond. Sci. Technol. **34**, 034001 (2019).
[7] Y. Irokawa et al., ECS J. Solid. State Sci, Technol. **13**, 085003 (2024).
[8] M. Hara, Mat. Sci. Semicond. Process. **196**, 109606 (2025).
[9] J. Uzuhashi et al., ECS J. Solid. State Sci, Technol. **14**, 085001 (2025).