Thu. Nov 6, 2025

Poster Session | Electron device, process, and characterization

Thu. Nov 6, 2025 5:00 PM - 6:30 PM JST | Thu. Nov 6, 2025 8:00 AM - 9:30 AM UTC Exhibition Hall (BF1)

[PS] Poster Session

[PS-01]

Depth profile analysis of charge trapping and chemical bonding states in Ni/SiO_2/AlN/GaN structures by voltage-applied AR-HAXPES

*Shunsuke Yamaguchi[1], Yoshiharu Kirihara[1], Yuichiro Mitani[1], Mariko Shimizu[2], Yukio Nakabayashi[2], Yosuke Kajiwara[2], Hiroshi Nohira[1] (1. Tokyo City University (Japan), 2. Toshiba Corporation, Corporate Laboratory (Japan))

[PS-02]

Anomalous Vg-Id Characteristics of GaN Power Device due to Ga penetration into AlN Interfacial Layers

*Yusuke Katsuro[1], Yoshiharu Kirihara[1], Shunsuke Yamaguchi[1], Makito Nishi[1], Mariko Shimizu[2], Yukio Nakabayashi[2], Yousuke Kajiwara[2], Hiroshi Nohira[1], Yuichiro Mitani[1] (1. Tokyo City University (Japan), 2. Toshiba Corporation, Corporate Laboratory (Japan))

[PS-03]

Effect of Forming Gas Annealing for 3C-SiC n-MOSFET

Rima Nishizaki[2], Dong Wang[2], *Keisuke Yamamoto[2,1] (1. Kumamoto University (Japan), 2. Kyushu University (Japan))

[PS-04]

IGZO Transistors with 700 °C Thermal Budget for Advanced DRAM Applications

*Nannan You[1,2], Tianhao Liao[1,2], Jiayi Wang[1,2], Yang Xu[1,2], Shengkai Wang[1,2] (1. Institute of Microelectronics of Chinese Academy of Sciences (China), 2. Chinese Academy of Sciences (China))

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Influence of Ar/O_2 ratio during IGZO deposition on the electrical characteristics of a-IGZO metal-insulator-metal diodes

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[PS-06]

Effect of annealing temperature on the electrical characteristics of Al/CuO/p-Si MOS capacitors

*Siang-Yi Hong[1], Xiao-Xuan Zeng[1], Pei-Hsuan Su[1], Yu-Hung Chen[1] (1. Department of Microelectronics Engineering, National Kaohsiung University of Science and Technology (NKUST) (Taiwan))

[PS-07]

Effects of Interface Formation Process on Tunneling Current Components of N-type $Ti_{0.3}Zn_{0.7}O_{1.3}$/P-type Si Stack Structure

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[PS-08]

Classical Molecular Dynamics Simulation of Ferroelectric Properties of a-HfO_2

*Jumpei Ohba[1], Sora Yamamoto[1], Yusuke Nishimura[1], Takunobu Watanabe[1] (1. Waseda University (Japan))

[PS-09]

Effects of Al Concentration and Annealing Method on Crystalline and Ferroelectric properties of Al:HfO_2 Thin Films

*Tomoya Mifune[1], Hideaki Tanimura[1,2], Yuma Ueno[2], Yusuke Tani[2], Yukiya Sano[1], Hironori Fujisawa[1], Seiji Nakashima[1], Ai I Osaka[1], Shinichi Kato[2], Takumi Mikawa[2] (1. Univ. of Hyogo (Japan), 2. SCREEN (Japan))

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Consideration on the Coexisting Positive- and Negative-Imprinted Ferroelectric Domains and Their Imprint-Recovery in Non-Doped HfO_2 MFM Capacitor

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Polarization Inversion in Hf-based Oxide Layer with High Si Content in MOS Structure

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[PS-12]

Effect of Plasma Treatment on Performance of AlScN-Based Ferroelectric Tunnel Junctions

*Yuki Yamada[1], Kazuki Goshima[1], Yoshiharu Kirihara[1], Ryouichi Kawai[1], Kuniyuki Kakushima[2], Hiroshi Nohira[1], Yuichiro Mitani[1] (1. Tokyo City University (Japan), 2. Institute of Science Tokyo (Japan))

[PS-13]

Study on Defect Generation in Ferroelectric AlScN from TDDB Statistical Point of View

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New SOD for Crack-Free Thick Film

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Profile-Based Modeling of AC Stress-Induced Degradation in SiON pMOSFETs

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New Insights into MOS Interface Degradation of pMOSFETs and nMOSFETs at Cryogenic Temperature

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High-Performance Ge FinFET CMOS Devices with Low-Temperature Supercritical Fluid Process after Post-Plasma Oxidation and Nitridation Treatments

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Fabrication and Performance Analysis of Sol-Gel NiO/Si 830nm Near-Infrared Photodetectors Deposited by Spin-Coating Process

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[PS-22]

New opportunity of GeSiSn/GeSn heterostructure for HEMT application

*Shota Torimoto[1], Mitsuo Sakashita[1], Masashi Kurosawa[1], Osamu Nakatsuka[1,2], Shigehisa Shibayama[1] (1. Grad. Sch. of Eng., Nagoya Univ. (Japan), 2. IMaSS, Nagoya Univ. (Japan))

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[1]Tokyo city Univ., [2]Toshiba Corporation, Corporate Laboratory
[1]1-28-1 Tamazutsumi, Setagaya-ku, Tokyo 158-8557, Japan
Email: g2581296@tcu.ac.jp /Phone +81-3-5707-0104

1. Introduction

In recent years, high-efficiency power conversion has been required in fields such as telecommunication base stations and data centers. To achieve this, it is expected that power devices using gallium nitride (GaN), a next-generation power device material, will offer higher performance [1]. In particular, GaN power devices with trench structures are expected to achieve both high integration and low loss. However, a major challenge is to solve reliability issues such as threshold change, which is believed to be caused by charge trapping in the dielectric film. To solve this problem, we have investigated the distribution and origin of the traps in the dielectric film by using voltage-applied angle-resolved hard X-ray photoelectron spectroscopy (AR-HAXPES), based on the changes in the photoelectron spectra before and after the application of voltage stress.

2. Experimental Procedure

Figure 1 shows the structure of the measured samples. These samples were measured using voltage-applied AR-HAXPES measurements at BL09XU [2] ($h\nu$ = 7933 eV) at SPring-8 with take-off angles (hereafter TOA) ranging from 12.7° to 67.3°. Photoelectrons from the inner shells of Al 1*s*, Si 1*s*, Ga 2*p*, N 1*s* and O 1*s* were measured. Here, the Ni electrode was grounded and voltage was applied to the GaN substrate. In the figures and tables, the voltage is indicated by the potential of the Ni electrode with respect to the GaN, so the polarity is opposite to the actual applied voltage.

3. Results and Discussion

Figures 2(a), (b), (c), and (d) show the photoelectron spectra of Ni 2*p*, Si 1*s*, Al 1*s*, and Ga 2*p* measured before and after applying 10 V voltage stress, respectively. Note that no voltage is applied during either measurement. Figures 2(b) and 2(c) show that the reaction occurred at the interface between SiO_2 and AlN, forming Si-N and Al-O. The binding energy of Ga 2*p* increases after voltage stress as shown in Fig. 2(d). This suggests that holes are trapped or electrons are de-trapped in the SiO_2/AlN layer due to voltage stress. The fact that the Ni 2*p* shift is not observed indicates that it is not a charge-up. The differences in the binding energies of photoelectrons from their respective inner-shell orbitals before and after the application of voltage stress are shown in Table 1. The large shift in Ga 2*p* and Al 1*s* means that charge trapping occurs in the AlN film and at the SiO_2/AlN interface. Table 2 shows the shift of binding energy from their initial binding energy when the applied voltage is 5 V, 7 V, and 10 V. Table 2 shows that the higher the applied voltage, the larger the binding energy shift. Figure 3 shows Ga 2*p* photoelectron spectra measured at various angles, normalized by total photoelectron intensity. The figure shows that the percentage of intensity from oxidized Ga increases as TOA decreases. This suggests that a part of Ga diffuses to the vicinity of the SiO_2/AlN interface. Figure 4 shows the TOA dependence of the intensity ratios of other photoelectron spectra on the Si 1s photoelectron intensity from the Si substrate (a) and the Ga 2p photoelectron intensity from the GaN substrate (b). From the figure, it can be seen that the angular dependence of Al 1*s*/Ga 2*p* on the GaN substrate is smaller than that on the Si substrate. This indicates that Ga diffuses into the AlN film, which is also consistent with the result in Figure 3. From the above, the origin of the charge trap is likely to be Ga diffused in AlN.

Acknowledgement

The synchrotron radiation experiments were performed at BL09XU of SPring-8 with the approval of Japan Synchrotron Radiation Research Institute (JASRI, Proposal Nos.2024B1695, 2025A1643, 2025A1574, 2025A1803, and 2025A1824).

References

[1] T. Avraham et al., Energies **18**, 1046 (2025). [2] A. Yasui et al., J. Synchrotron Radiat. **30**, 1013 (2023).

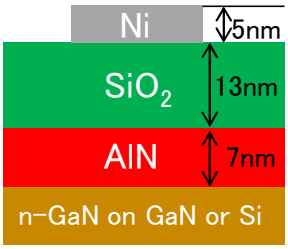

Fig. 1 Schematic structure of samples.

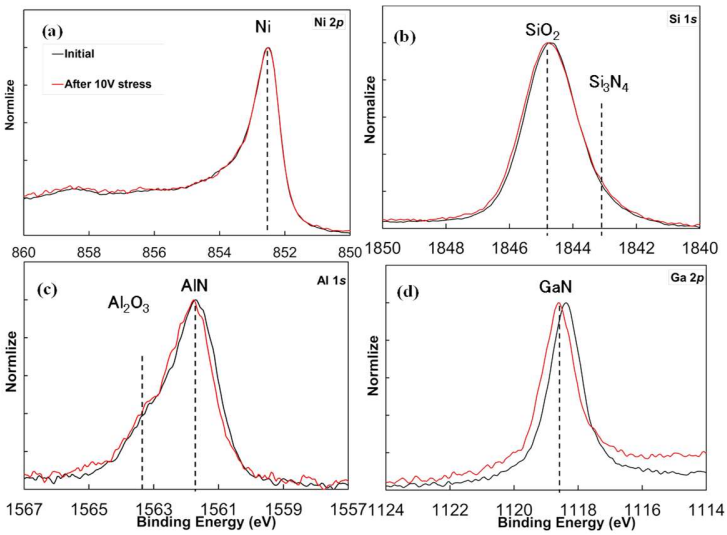

Fig. 2 (a) Ni 2*p*, (b) Si 1*s*, (c) Al 1*s*, and (d) Ga 2*p* photoelectron spectra measured by HAXPES, respectively.

Table 1 Binding energies of Si 1*s*, Al 1*s* and Ga 2*p* photoelectrons before and after applying voltage stress and the amount of change (Δ V) after applying stress.

Sample condition	Binding Energy (eV)		
	Si 1*s*(SiO_2)	Al 1*s*(AlN)	Ga 2*p*(GaN)
Initial	1844.735	1561.664	1118.402
After 10V stress (Δ V)	1844.763 (0.028)	1561.790 (0.126)	1118.627 (0.225)

Table 2 Stress voltage dependence of the change in binding energy of Si 1*s*,Al 1*s* and Ga 2*p* photoelectrons.

Sample condition	Amount of change Δ V (eV)		
	Si 1*s*(SiO_2)	Al 1*s*(AlN)	Ga 2*p*(GaN)
After-5V stress	0.018	0.073	0.164
After 7V stress	0.019	0.119	0.189
After10V stress	0.028	0.126	0.225

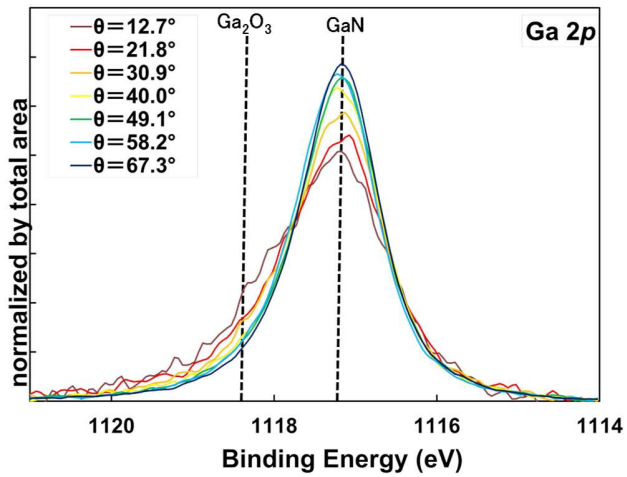

Fig. 3 TOA dependence of Ga 2*p* photoelectron spectra. Here, the height is normalized by the total spectral area.

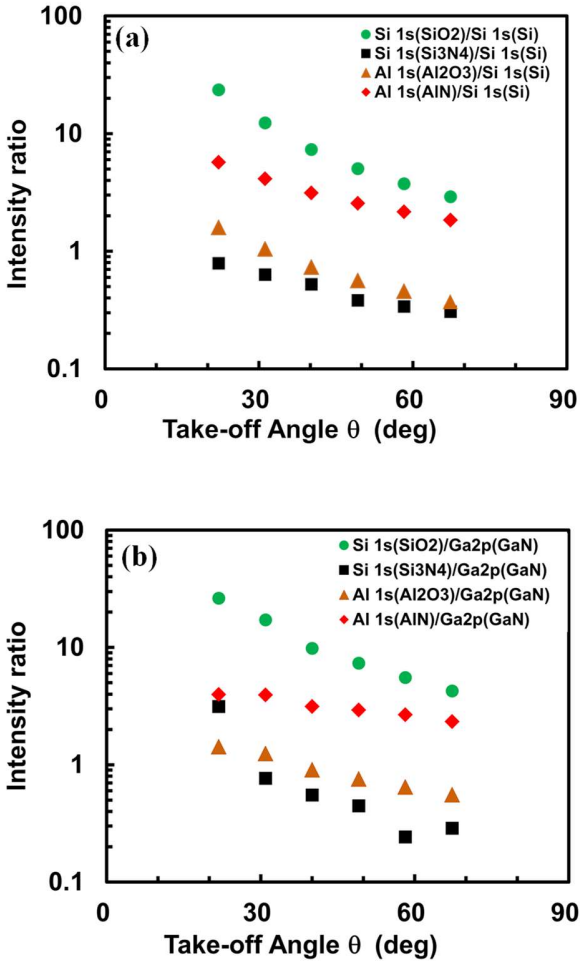

Fig. 4 TOA dependence of the photoelectron spectral intensity ratio normalized by the photoelectron intensity from the substrate. Here, (a) is for Si substrate and (b) is for GaN substrate.

Anomalous Vg-Id Characteristics of GaN Power Device due to Ga penetration into AlN Interfacial Layers

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Email: g2481225@tcu.ac.jp / Phone: +81-3-5707-0104

1. Introduction

GaN MOSFETs are promising power devices due to their high breakdown voltage and fast switching speed. In recent, introducing an AlN interfacial layer (IL) between the gate insulator and GaN channel has been reported to enhance mobility and suppress Vth variation by suppressing Ga penetration [1][2]. However, the device exhibited anomalous subthreshold swing (SS) degradation under negative bias stress as shown in Fig.1. It is also imperative to ensure the stability of the threshold voltage (Vth) to guarantee reliable operation. Therefore, in this study, we investigate the physical origin of this anomalous SS behaviour.

2. Experimental Procedure

A schematic cross-sectional view of the device structure is shown in Fig. 2. The channel width (W) and length (L) of the device used in this study are 20 μm and 1 μm, respectively, with an AlN interfacial layer of 3 nm.

3. Results and Discussion

Fig. 3 shows the Id–(Vg–Vth) characteristics of the device under three conditions: initial (before stress), post-stressed (after applying Vg = –15 V for 256 s), and after stress removal, where the Id–Vg curve was re-measured without applying stress. After the stress, the Id-Vg curve shows an anomalous degradation of the subthreshold swing (SS). On the contrary, after the gate voltage are turned off the Id-Vg characteristics are recovered immediately, the SS almost coincides with that observed in the initial Id-Vg curve. This result indicates the contribution of the carrier trapping / detrapping defects as schematically shown in Fig. 4. Under negative gate bias stress, the carriers captured in defect energy levels within the AlN layer are released, resulting in a negative shift in Vth. Subsequently, during the recovery phase, the carriers are re-trapped, which results in the recovery of the Id-Vg curve. According to the HAXPES measurement, it is inferred that the defects are attributable to the penetration of Ga into the AlN layer [4]. That is, the existence of these carrier trapping / detrapping in the AlN layer may be related to the anomalous Id–Vg characteristics observed after stress as shown in Fig. 1. To verify this hypothesis, we performed the single-point fast BTI measurements while minimizing recovery during the measurement. The measurement sequence of the fast BTI method is shown in Fig. 5. Fig. 6 shows the comparison between the ΔId by using the fast BTI measurement and that by using the full-sweep IV measurement. By the full-sweep IV method, ΔId values are smaller compared to those by the fast BTI method. This result indicates that the recovery during the full-sweep IV measurement caused by fast carrier trapping / detrapping occurs. Based on these results, it is inferred that the transient carrier trapping during the Vg sweep causes the anomalous SS degradation [5]. Fig. 7 presents schematic diagrams for the anomalous SS degradation due to transient carrier trapping during full-sweep IV measurement. When negative bias stress is applied, electrons are emitted and Vth shifts in the negative direction, but during the Vg sweep, transient electron re-trapping occurs, which leads to apparent SS degradation.

4. Conclusions

This study investigated the origin of anomalous SS degradation observed in GaN MOSFETs with an AlN interlayer under negative bias stress. Full-sweep IV measurements showed significant SS degradation, but Fast BTI revealed that it was caused by transient carrier trapping during measurement. The observed recovery behaviour also suggests fast trap/detrap dynamics in the AlN layer. These findings highlight the need to consider measurement-induced effects for the accurate reliability measurement of GaN MOSFETs.

References

[1] Y. Kajiwara et al., ISPSD. 32, 302 (2020).[2] K. Ito et al., IEDM. (2023).[3] X. Garros et al., IEEE IRPS, 2018.[4] S. Yamaguchi et al., to be presented in IWDTF-2025. [5] Y. Miyaki et al., IEEE IMFEDK, 2024.

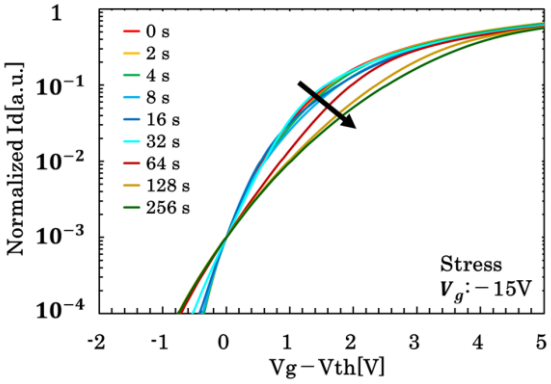

Fig.1. Stress time evolutions of Id-Vg characteristics of GaN MOSFETs measured at Vd = 1 V. Negative gate stress of Vg = –15 V are applied.

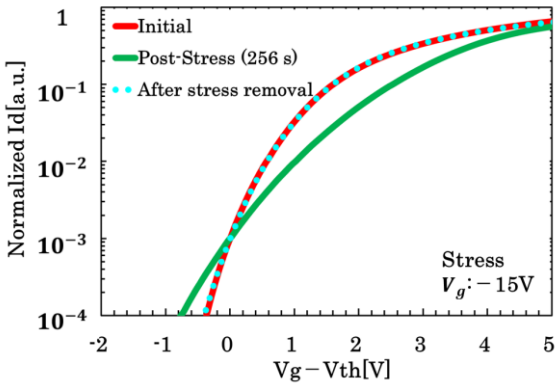

Fig.3. Comparing Id-Vg characteristics prior to stress and following negative bias stress (Vg = –15 V) for 256 sec, and recovered after stress removal.

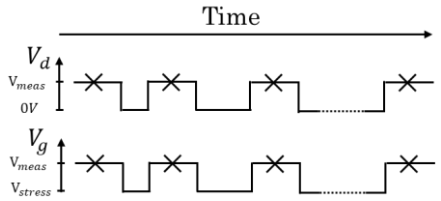

Fig.5. Measurement sequence of Fast BTI method using single-point Id measurement.

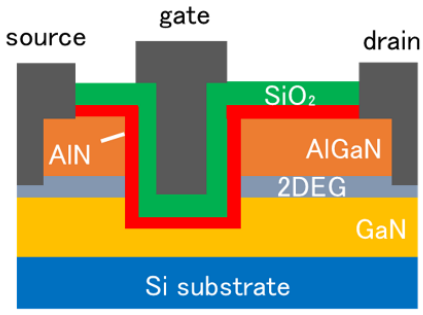

Fig. 2. Schematic cross-sectional image of GaN-MOSFETs (W/L = 20/1 μm), where 2DEG denotes a two-dimensional electron gas.

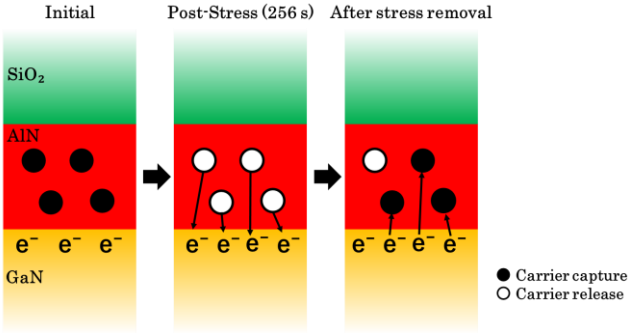

Fig.4. Schematic diagram of physical model for initial, post-stressed, and recovered Id-Vg characteristics.

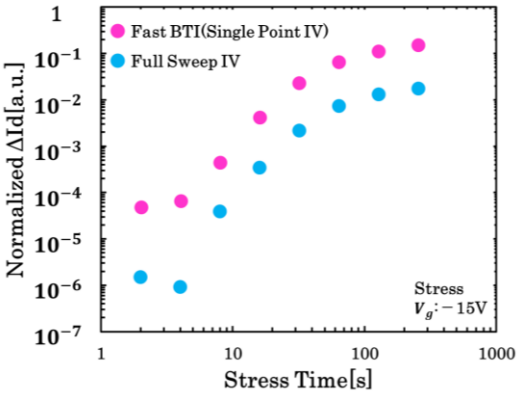

Fig.6. Δ Id as a function of stress time obtained by full sweep IV comparing to that by Fast BTI measurement.

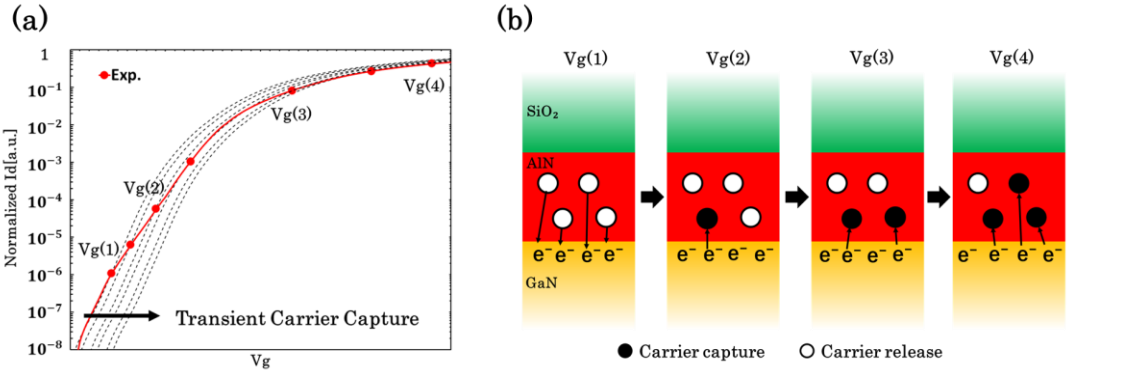

Fig.7. (a) Positive shift of Id-Vg characteristics due to electron trapping to generated bulk traps (*i.e.* transient carrier capture). When electron trapping increases transiently as increasing Vg, Id-Vg curve gradually shifts to the positive direction, where the dashed lines schematically illustrate Id–Vg curves without trapping at each point. (b) Schematic diagram of physical model explaining the mechanism of transient carrier trapping and its impact on the observed degradation behavior in SS.

Effect of Forming Gas Annealing for 3C-SiC n-MOSFET

Rima Nishizaki[1], Dong Wang[2], and Keisuke Yamamoto[2,3]
[1]Interdisciplinary Graduate School of Engineering Sciences, Kyushu University
[2]Faculty of Engineering Sciences, Kyushu University
6-1, Kasuga-koen, Kasuga, Fukuoka 816-8580, Japan
[3]Research and Education Institute for Semiconductors and Informatics, Kumamoto University
2-39-1, Kurokami, Chuo-ku, Kumamoto, 860-8555, Japan
Email: yamamoto.keisuke.380@cs.kumamoto-u.ac.jp / Phone: +81-96-342-3591

1. Introduction

Silicon carbide (SiC) has a high breakdown electric field and a wide bandgap, which are advantages for realizing high-efficiency power devices and devices that can operate at high temperatures. Among the polytypes of SiC, high-quality (111)-oriented cubic SiC (3C-SiC) can be grown epitaxially on Si (111) substrates [1]. For the application of 3C-SiC to electronic devices, the formation of an insulating film with excellent interfacial properties is essential for both MOS gate dielectrics and surface passivation layers. We have previously reported that sputter-deposited SiO_2 combined with a plasma-oxidized interfacial layer (IL) provides high interfacial quality on 3C-SiC, and MOSFETs employing this gate stack exhibit a high field-effect mobility (μ_{FE}) of 131 cm^2/Vs [2,3]. In this study, we introduce forming gas annealing (FGA) into the gate stack process [4]. As a result, improvements in device performance, particularly μ_{FE}, were obtained for 3C-SiC MOSFETs.

2. Experimental Procedure

The substrate was (111)-oriented, boron-doped p-type 3C-SiC epitaxially grown on a p-Si (111) wafer, with a hole concentration on the order of 10^{15} cm^{-3}. The fabrication procedure is outlined in Fig. 1. All MOSFETs were designed with a current flow direction of <110>. Source/drain (S/D) regions were formed through a multistep nitrogen ion implantation process (20–70 keV) using a patterned SiO_2 mask at 500 °C, followed by activation annealing at 1300 °C. The gate stack was subsequently formed by introducing an electron cyclotron resonance (ECR) plasma-oxidized IL and sputter-deposited SiO_2 (30 nm). Post-deposition annealing (PDA) was conducted in forming gas (FG, Ar:H_2 = 9:1) at 400 °C for 30 min. Thermally evaporated Al was used as the gate and S/D electrodes, followed by contact annealing (CA) in FG at 300 °C. For comparison, MOSFETs treated N_2 PDA and CA instead of FG annealing were also prepared.

3. Results and Discussion

Figure 2 shows the transfer characteristics (drain current I_D, source current I_S vs gate voltage V_G) of the fabricated MOSFET with FG annealing (FGA) in this study. It shows a typical MOSFET operation curve with a clear ON/OFF transition. Figure 3 shows the output characteristics (I_D vs drain voltage V_D) of the MOSFET with N_2 annealing and FGA. The MOSFET with FGA exhibits higher current drivability than the MOSFET with N_2 annealing. Figure 4 shows μ_{FE} of the fabricated MOSFETs with (solid line) and without (dotted line) FGA. By introducing the FGA, peak μ_{FE} was improved, typically at a low V_G corresponding to a low electric field region. The peak μ_{FE} of 160 cm^2/Vs is 22% higher than our previous study (131 cm^2/Vs) with N_2 annealed gate stack [3]. To clarify the origin of ON-current enhancement, we compare parasitic resistance and channel resistance. Figure 5 shows the device total resistance vs channel length plots for the devices with FG and N_2 annealing. The parasitic resistances, corresponding to the y-axis interception of the fitting line, remain unchanged when the PDA ambient is altered. On the other hand, channel resistance (R_{ch}), corresponding to the slope of the fitting line, is reduced by introducing FGA. These results (Figs. 4 and 5) suggest that the Coulomb scattering at the low electric field is well suppressed due to the improvement of the gate stack quality. Similar to the previous study on the FGA effect for a MOS capacitor with CVD-SiO_2 on 3C-SiC [4], FGA is also efficient for plasma-oxidized and sputter-deposited SiO_2, thereby improving μ_{FE}.

4. Conclusions

We confirmed the effectiveness of the FGA for 3C-SiC n-MOSFET. FGA is effective in reducing the channel resistance under on-state conditions. The peak μ_{FE} of 160 cm^2/Vs for the MOSFET with FGA is 22% higher than that of the N_2 annealed MOSFET. These results will be helpful guidelines for various 3C-SiC device applications.

Acknowledgements

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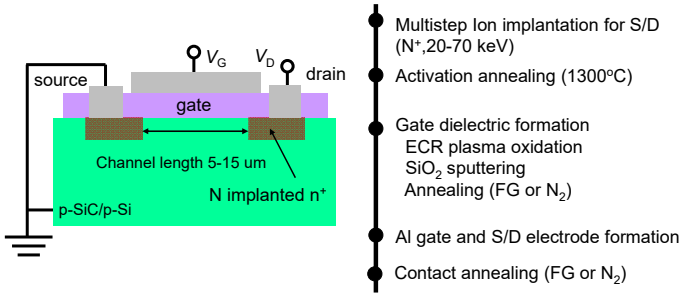

Fig. 1 Cross-sectional illustration and the fabrication procedure of 3C-SiC n-MOSFET in this study.

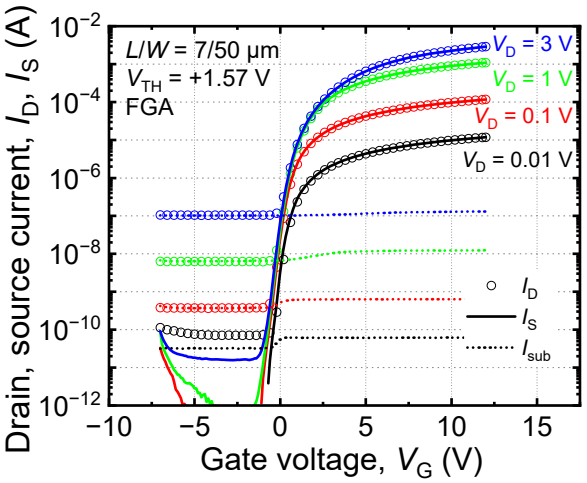

Fig. 2 Transfer characteristics of 3C-SiC n-MOSFET with FGA.

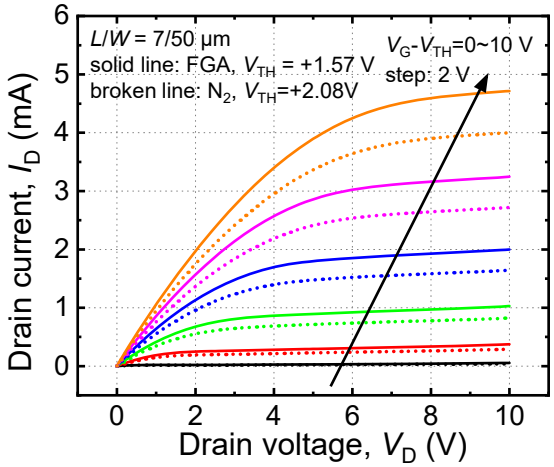

Fig. 3 Output characteristics of 3C-SiC n-MOSFETs with FGA and N_2 annealing.

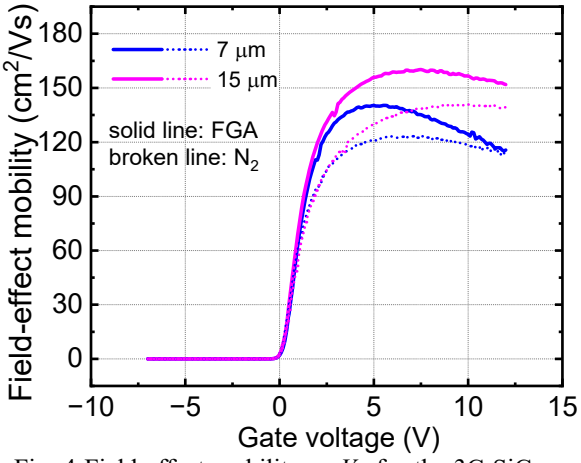

Fig. 4 Field-effect mobility vs V_G for the 3C-SiC n-MOSFETs with FGA and N_2 annealing.

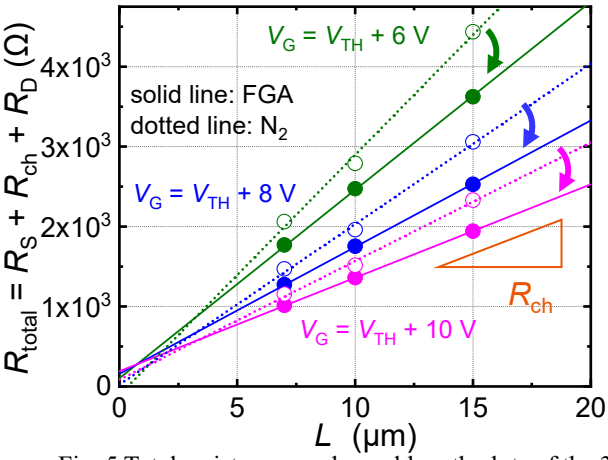

Fig. 5 Total resistance vs channel length plots of the 3C-SiC n-MOSFET for channel resistance calculation.

IGZO Transistors with 700 °C Thermal Budget for Advanced DRAM Applications

Nannan You[1,2#], Tianhao Liao[1,2#], Jiayi Wang[1,2], Yang Xu[1,2], Shengkai Wang[1,2*]

[1]State Key Laboratory of Fabrication Technologies for Integrated Circuits, Chinese Academy of Sciences, Beijing, 100029, China; [2] Institute of Microelectronics of Chinese Academy of Sciences, Beijing 100029, China;

[*]E-mail: wangshengkai@ime.ac.cn; [#]Equally contributed

1. Introduction

The 1T1C architecture utilizing AOS materials provides high storage density and low power consumption. Achieving its potential requires overcoming the high thermal budget (~700 ºC) needed for capacitive processes during the integration [1-3]. Key obstacles include leakage from crystallized high-k dielectrics and performance degradation due to interfacial atomic interdiffusion. In this work, by co-engineered HfAlO gate dielectric with an Al_2O_3 interlayer, we demonstrate amorphous IGZO transistors that withstand 700 °C with superior performance.

2. Experimental Process

Fig. 1(a) shows the device structure. IGZO transistor fabrication began with atomic layer deposition (ALD) at 250 ºC of a 25 nm HfAlO dielectric layer on n^+-Si, followed by a 1 nm Al_2O_3 interlayer. A 5-min N_2 anneal at 500 ºC homogenized the HfAlO stack. A 15 nm IGZO channel and 25 nm ITO source/drain electrodes (defined by shadow mask) were deposited via RF sputtering. Finally, a 45-min anneal at 400 °C was performed in the air. The study compared dielectric materials (HfAlO, HfSiO, HfO_2, Al_2O_3) and interlayers (HfO_2, Al_2O_3, SiO_2). A 700 ºC N_2 anneal was applied to simulate the capacitor process temperature.

3. Results and Discussion

The interlayer should ensure interfacial compatibility while suppressing dielectric-channel interdiffusion. Thermodynamic and ab-initio molecular dynamics (AIMD) simulations (data not shown) indicated that Al_2O_3 maintains a stable electronic structure, crucial for electrical consistency. Fig.1(b) TEM/EDS confirmed the Al_2O_3 interlayer effectively suppressed interdiffusion. Experimentally, IGZO transistors with Al_2O_3 interlayer achieved the steepest SS (96 mV/dec), as shown in Fig. 2(b),validating its superior performance and aligning with theoretical predictions.

Achieving a high thermal budget necessitates dielectrics that are uniform, amorphous, and possess a high crystallization temperature. TEM/EDS revealed uniform dielectric composition but greater Si diffusion than Al into the IGZO after 700°C annealing (data not shown), generating defects. While IGZO transistors exhibited initially comparable performance (Fig. 3a), 700 °C annealing caused severe degradation in HfSiO devices. In contrast, devices with HfAlO maintained stable performance and demonstrated superior bias stress stability (Fig. 3b). HfAlO's uniformity, high *k*, and thermal stability establish it as the superior gate dielectric.

To validate the co-engineered gate stack approach, we fabricated IGZO transistors with HfAlO dielectric-Al_2O_3 interlayer (HfAlO-Al) stacks. Devices subjected to 0-7 min annealing (Fig. 4a) showed progressive positive V_{th} shifts while maintaining relatively stable SS and minimal gate leakage. Critical parameter analysis (Fig. 4b) revealed optimal performance at 5 min: the steepest SS (84 mV/dec) and exceptional stability (+17 mV PBS, -7 mV NBS @±3.8 MV/cm for 2000 s). Therefore, through co-engineering, the HfAlO-Al IGZO transistor achieves the 700 ºC thermal budget for 5 min with superior performance.

4. Conclusions

This work presents the 700 °C-compatible IGZO transistors, enabled by a co-engineered HfAlO-Al gate stack. This material provides a high *k* dielectric, a thermally stable interlayer, and a sharp interface with suppressed diffusion. Devices show exceptional stability, providing a new solution for high-density 1T1C integration.

Acknowledgements

This work was supported by the International Partnership Program (for Future Network) of the Chinese Academy of Sciences Grant No. 102GJHZ2022066FN.

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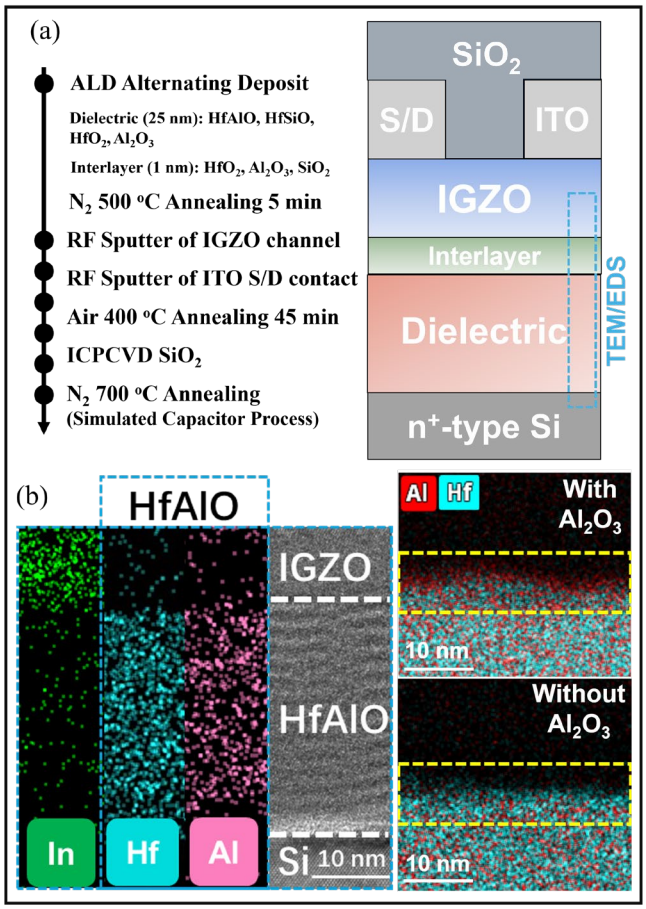

Fig. 1 (a) Key process flow and device structure, (b) TEM cross-sectional image and EDS mapping of IGZO taransitors with and without Al_2O_3 interlayer.

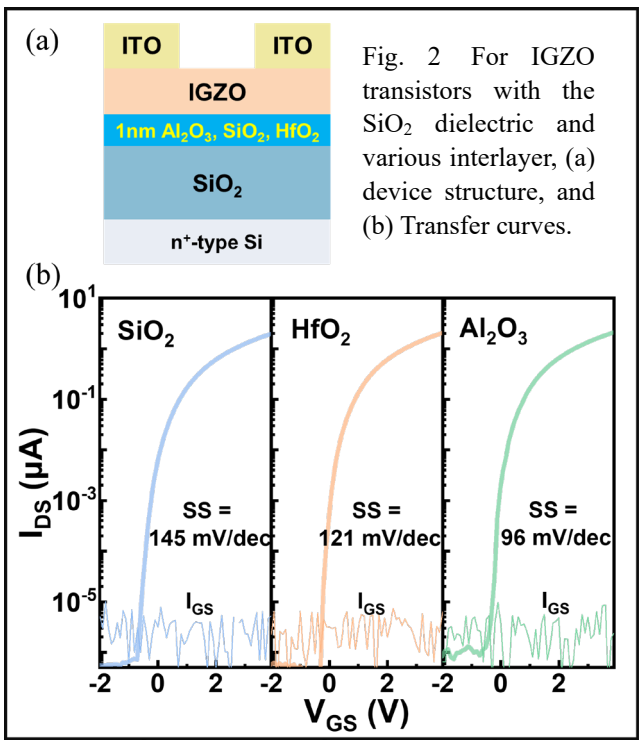

Fig. 2 For IGZO transistors with the SiO_2 dielectric and various interlayer, (a) device structure, and (b) Transfer curves.

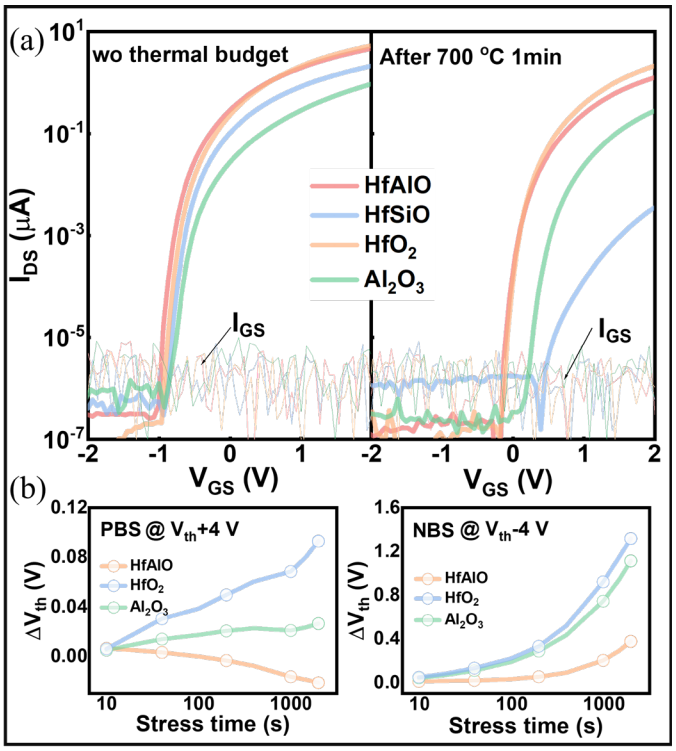

Fig. 3 For IGZO transistors with various dielectrics, (a) Transfer curves and (b) Bias stress stability.

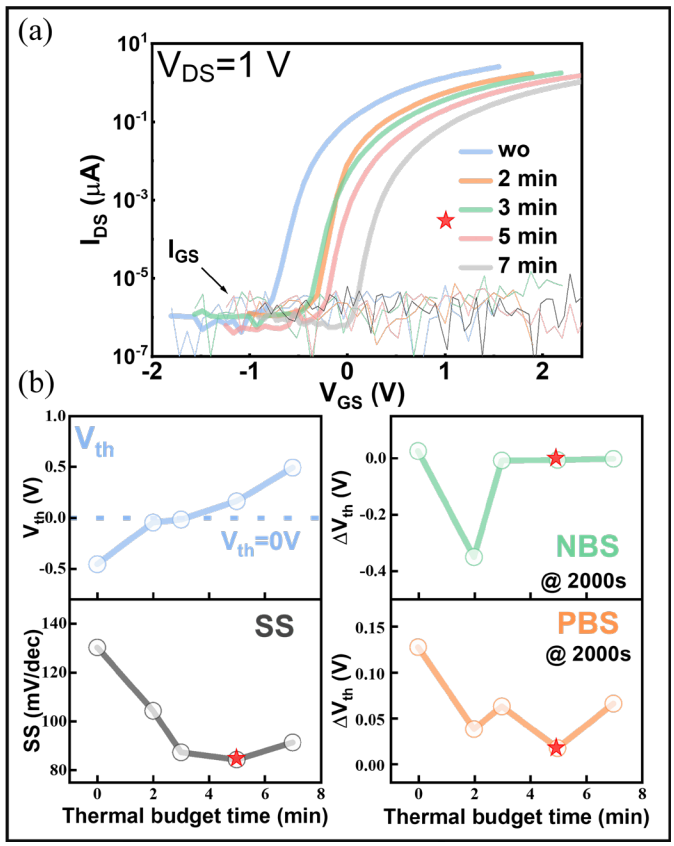

Fig. 4 For IGZO transistors with HfAlO-Al gate dielectric at 700 °C thermal budget, (a) Transfer curves and (b) Extracted critical parameter vs. thermal budget time.

Influence of Ar/O_2 ratio during IGZO deposition on the electrical characteristics of a-IGZO metal-insulator-metal diodes⁻

Chih-An Chen, Bai-Jun Guo, Chang-Yi Yen, Yu-Hung Chen
Department of Microelectronics Engineering, National Kaohsiung University of Science and Technology
Kaohsiung City 811213, Taiwan
Email: yhchen@nkust.edu.tw

1. Introduction

This study employed RF sputtering to fabricate metal–insulator–metal (MIM) tunneling diodes, exploring the feasibility of amorphous indium gallium zinc oxide (a-IGZO) as the insulating layer beyond its conventional applications in displays and touch panels. The oxygen flow ratio during deposition and the post-annealing temperature were systematically varied, and the electrical characteristics were analyzed through device measurements. For the first time, key MIM diode parameters [1] such as asymmetry, nonlinearity, and responsivity were introduced for a-IGZO–based devices, along with a ideality factor (N) to evaluate performance. Comparative analysis was conducted to assess device characteristics under different oxygen flow and annealing conditions.

2. Experimental Procedure

FTO and glass substrates were cut to size and sequentially cleaned in acetone, isopropanol, and deionized water by ultrasonic agitation (10 mins each), followed by N_2 drying and baking at 100 °C. a-IGZO thin films were deposited by RF sputtering at a base pressure of 5×10^{-6} Torr. The IGZO film was deposited as a function of the gas flow rate of argon and oxygen (Ar/O_2) of 39.2:0.8, 38:2, and 36:4 sccm, respectively. Deposition parameters were adjusted to obtain the desired thickness (~10 nm), which was verified by Alpha Step measurements. The FTO/a-IGZO structures were then annealed by rapid thermal annealing (RTA) at 5×10^{-3} Torr, and Al top electrodes (~100 nm) were subsequently deposited by thermal evaporation under 5×10^{-6} Torr, forming the FTO/IGZO/Al devices. The electrical properties were characterized by I–V measurements, Hall effect, and four-point probe analysis.

3. Results and Discussion

Figure 2 shows that the I–V characteristics depend on the argon/oxygen (Ar/O_2) flow ratios of 39.2:0.8, 38:2, and 36:4 sccm. At low oxygen (Ar/O_2 = 39.2:0.8), the annealed device shows nearly Ohmic behavior (see Fig. 2a), whereas increasing oxygen to 2 sccm yields typical MIM diode behavior, with the highest ON/OFF ratio obtained at Ar/O_2 = 36:4. In figures 3a–3c shows that the maximum asymmetry values at room temperature are 0.97 and 87.16, whereas at 500 °C they are 26.83 and 536.57, yielding asymmetry rising magnification of 89.69 and 20 (see Fig. 3d). This indicates that the asymmetry is highly sensitive to temperature. However, both Ar/O_2 of 39.2:0.8 and Ar/O_2 of 36:4 show asymmetry degradation at higher bias(see Fig. 3a and 3c), which correlates with larger ideality factors (N = 5.84 and 7.96) and may result from microcrystallization or oxygen release in a-IGZO [2]. Table I. and Figure 5 indicate that larger ideality factors correspond to stronger nonlinearity, consistent with the defect-rich conditions at Ar/O_2 = 39.2:0.8 and 36:4. In contrast, samples with fewer defects show weaker correlation. Turn-on voltage is almost unaffected at lower oxygen flow but becomes more sensitive at higher oxygen flow, while excessive oxygen (Ar/O_2 of 36:4) reduces nonlinearity. Finally, Figure 5 shows that the maximum responsivity is achieved at Ar/O_2 of 36:4 at room temperature.

4. Conclusions

Device performance improves as oxygen flow reduces defects, but excessive oxygen introduces interface states and instability. Annealing enhances performance up to an optimum level, beyond which a-IGZO degrades. The best condition is achieved at Ar/O_2 of 36:4 with annealing at 300 °C.

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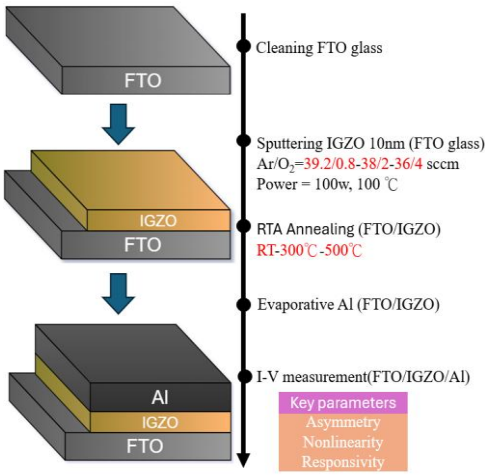

Fig. 1 Fabrication flow of FTO/a-IGZO/Al MIM diodes and key electrical parameter analysis.

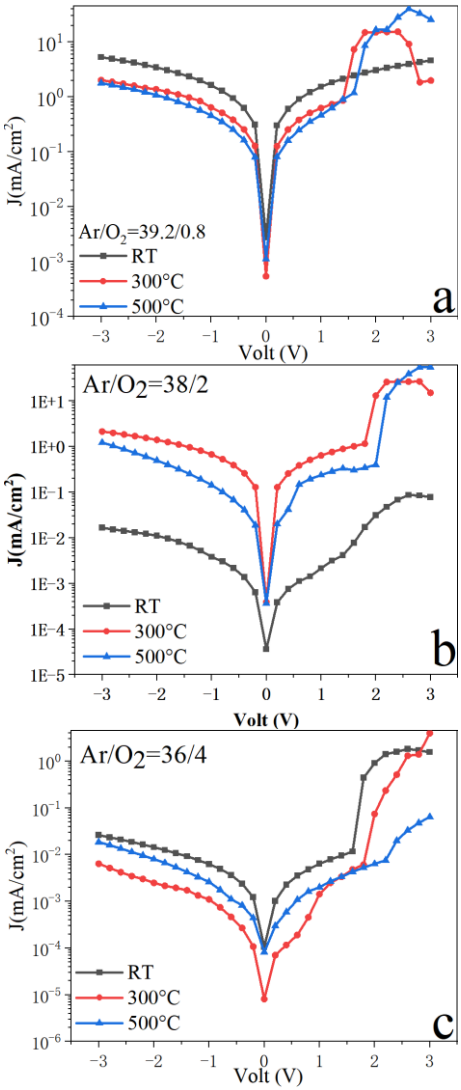

Fig. 2 I–V characteristics of the Ar/O_2-sputtered IGZO MIM devices with respect to various annealing temperatures.

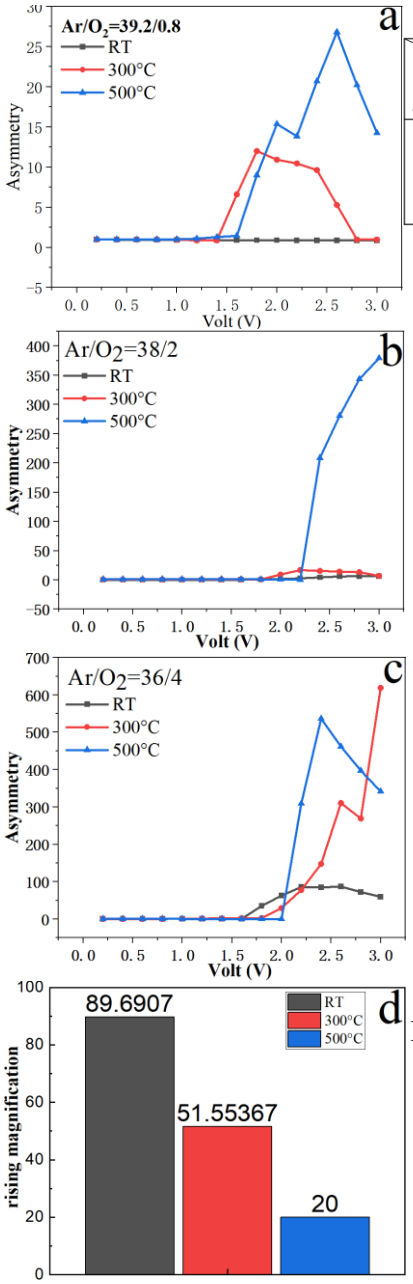

Fig. 3 Asymmetry at different oxygen flow rates and annealing temperatures : (a) Ar:39.2 O_2:0.8 (b) Ar:39, O_2:2 (c) Ar:36,O_2:4 and (d) comparison charts for asymmetry rising magnification.

Table I Nonlinearity maximum

Ar/O_2 flow / Anneal temp	Ar: 39.2 O_2= 0.8	Ar: 38 O_2= 2	Ar: 36 O_2= 4
RT	1.038	9.597	295.205
300˚C	52.468	92.057	99.954
500˚C	49.701	289.784	19.322

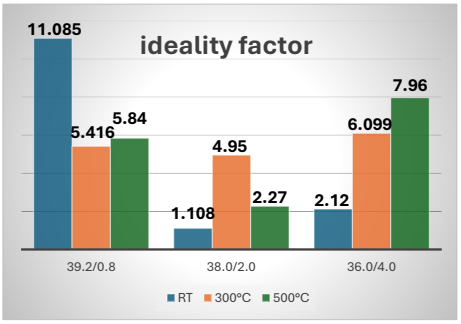

Fig. 4 Ideality factor of the FTO/a-IGZO/Al MIM diode.

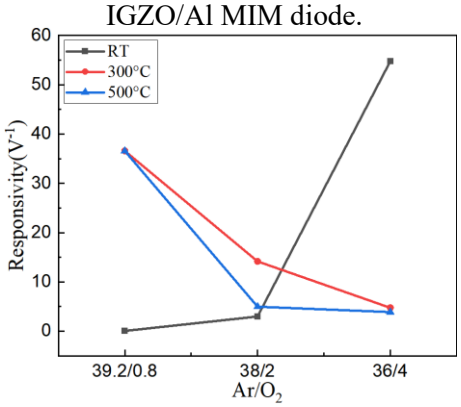

Fig. 5 Responsivity of different oxygen flow rates and annealing temperatures of maximum.

Effect of annealing temperature on the electrical characteristics of Al/CuO/p-Si MOS capacitors

Siang-Yi Hong, Xiao-Xuan Zeng, Pei-Hsuan Su, Yu-Hung Chen
Department of Microelectronics Engineering, National Kaohsiung University of Science and Technology, Kaohsiung City 811213, Taiwan
Email: yhchen@nkust.edu.tw

1. Introduction

Copper oxide (CuO) owing to its natural abundance, non-toxicity, low cost, and promising electrical and optical properties. CuO is a p-type semiconductor with a monoclinic crystal structure and a bandgap ranging from 1.2 to 2.16 eV. Various deposition techniques, including chemical bath deposition, pulsed laser deposition, and radio frequency (RF) magnetron sputtering, have been employed for the fabrication of CuO thin films.[1] Among these methods, sputtering is widely recognized for producing semiconductor thin films of superior quality, particularly in terms of reproducibility and reliability. The impact of different annealing temperatures on the structural, chemical, optical, and MOS properties of radio frequency (RF) magnetron sputtered CuO passivation layers on high-performance Si-based MOS capacitors was reported in this work.

2. Experimental Procedure

The copper oxide films were grown at room temperature by reactive magnetron sputtering. By using acetone, ethanol, and deionized water, the silicon substrates were rinsed ultrasonically. By blowing nitrogen gas, these substrates were dried in case of deposition. First, 375 nm of aluminum was deposited on the backside of the p-Si and annealed in air at 500 °C for 2 minutes to serve as the back electrode. In the experiment, a CuO target of 3 inches with 99.99% purity was used. The rotation rate of 12 rpm was fixed during the deposition. The vacuum chamber was evacuated until the base pressure reached 20 mTorr. Mixed argon–oxygen was used as the reactive gas. The oxygen flow rate was 0.05sccm, while the argon flow rate was kept at 20 sccm. Then, circular electrodes with a diameter of 0.15 mm and a thickness of 150 nm were deposited by thermal evaporation. This work using a deposition recipe of room temperature and studied the effect of post-deposition annealing temperature at 150°C, 250°C, and 350°C for 30 minutes on the electronic properties.(see Fig.1)

3. Results and Discussion

The Tauc plot, **C–V** and **I–V** characteristics of the fabricated Al/ CuO/ p-Si structures were investigated.

The optical gaps can be determined from the Tauc plot ($(\alpha h\nu)^{1/2}$ vs Eg). This is in contrast to the electronic band gap of the material since the presence of shallow defect states can change the optical gap . The optical band gap is found to decrease substantially, moving from 1.61 eV for the as-deposited film to 1.51 eV for the film annealed at 350 °C. For the annealing temperature at 150 °C and 250 °C, the value is mostly insensitive. [2][3] (see Fig.2)

All electrical measurements were performed at room temperature using an Agilent B1500A semiconductor device analyzer. The dc bias voltage swept from −2 to 4 V, whereas the C–V measurements were performed in the frequency of 1 MHz.

Based on the I–V measurements, it was observed that the sample annealed at 150°C exhibited the lowest leakage current of 3.97×10^{-9} A. An overall decrease in rectification ratio is observed with higher annealing temperatures, except at 350°C where an upward trend occurs. By using Cheung's function [4], the barrier heights were found to be 0.74 eV for both the as-deposited sample and the sample annealed at 150°C, while the values were 0.79 eV and 0.76 eV for the samples annealed at 250°C and 350°C, respectively.(see Fig.3)

The C–V characteristics revealed that the sample annealed at 350°C exhibited a higher capacitance value of 1.95×10^{-10} F.[5](see Fig.4)

4. Conclusions

Copper oxide thin films were successfully grown by magnetron sputtering, and the measurement results agreed well with the experimental predictions. Al/CuO/p-Si structure were fabricated and analyzed through optical and electrical measurements. The optical band gap decreased from 1.61 eV (as-deposited) to 1.51 eV after annealing at 350 °C, suggesting the influence of defect states.I–V analysis showed the lowest leakage current (3.97×10^{-9} A) at 150 °C, while the rectification ratio decreased with annealing but slightly recovered at 350 °C. Cheung's method revealed barrier heights ranging from 0.74 to 0.79 eV depending on the annealing temperature. From the C–V

measurements, it can be concluded that after annealing, the shift trend became more consistent, and a more pronounced increase in capacitance was observed for the sample annealed at 350°C.

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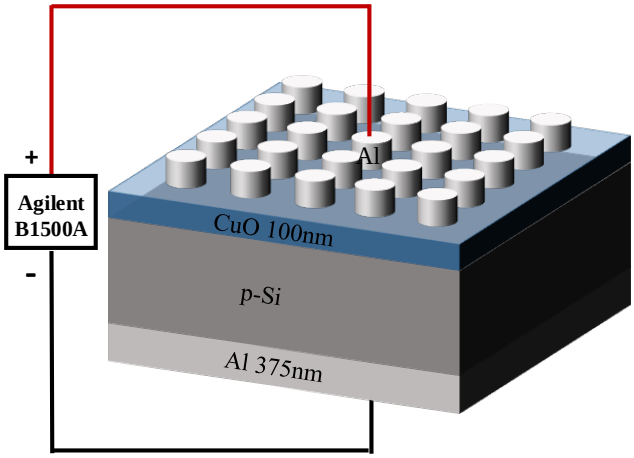

Fig. 1 Shows the schematic diagram of the device structure.

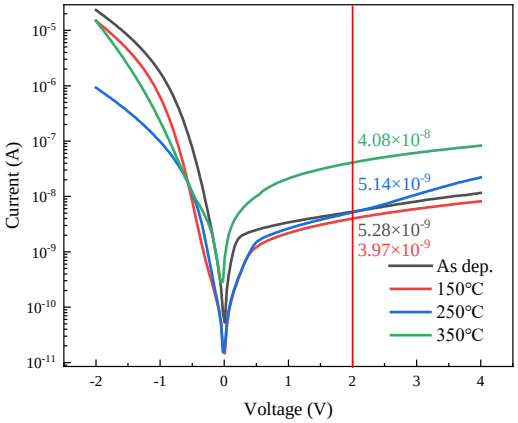

Fig. 3 I-V plot of annealing temperature of 150°C , 250°C , 350°C and non-annealing.

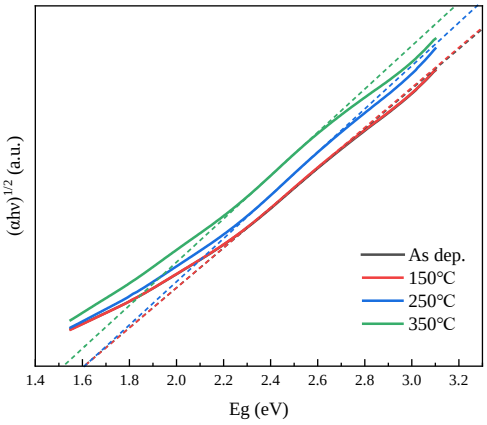

Fig. 2 Tauc plots of annealing temperature of 150°C, 250°C, 350°C and non-annealing.

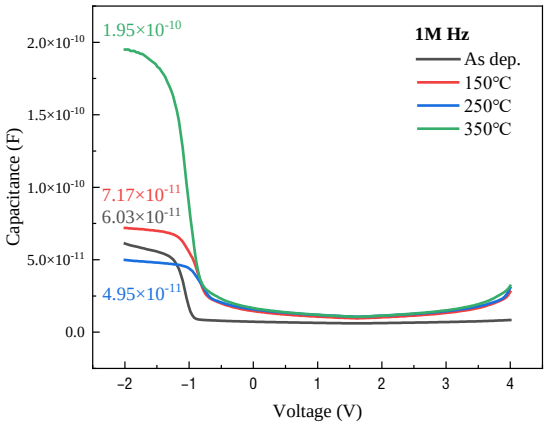

Fig. 4 C-V plot of annealing temperature of 150°C , 250°C , 350°C and non-annealing.

Effects of Interface Formation Process on Tunneling Current Components of N-type $Ti_{0.3}Zn_{0.7}O_{1.3}$/P-type Si Stack Structure

Kenta Ogawa[1,2*], Toyohiro Chikyow[2], Atsushi Ogura[1,3] and Takahiro Nagata[2,1*]
[1] Graduate School of Science and Technology, Meiji University, Kawasaki, Kanagawa 214-8571, Japan
[2] National Institute for Materials Science (NIMS), Tsukuba, Ibaraki 305-0044, Japan
[3] Meiji Renewable Energy Laboratory, Meiji University, Kawasaki, Kanagawa 214-8571, Japan
*E-mail: ce241031@meiji.ac.jp, NAGATA.Takahiro@nims.go.jp

1. Introduction

Currently, electrical devices are required to reduce power consumption and increase functionality. Tunnel field effect transistors (TFETs) allow devices to reduce power consumption and operate quickly thanks to achieve subthreshold swing values (S.S.) smaller than 60 mV/dec which is the theoretical limit of conventional Si-MOSFETs, by taking advantage of the electron tunneling effect [1,2]. Recently, bilayer structure TFETs combining amorphous ZnSnO, a n-type oxide semiconductor (n-OS), and Si, a p-type group IV semiconductors, have been proposed. It was effective that channel layer has amorphous structure to improve the performance of TFETs, because of the high film uniformity. However, further reduction of S.S. have been disturbed by the existence of oxygen defects and tail-states near conduction band minimum on oxide semiconductors due to the amorphous structure [3]. To resolve this trade-off, we have investigated $Ti_{0.3}Zn_{0.7}O_{1.3}$ which is ZnO-based solid solution with Ti having high oxygen bond dissociation energy. As a result, we confirmed that the $Ti_{0.3}Zn_{0.7}O_{1.3}$ film with an initial TiO_2 layer in a TiO_2/ZnO multiple stacked structure formed the most uniform unintentional interfacial SiO_2 layer [4]. Our next challenge is to investigate the effects of differences in interface structure on tunneling current characteristics and indicate the relationship. In this study, we report the results of evaluating the temperature and electric field dependence of the I-V characteristics of $Ti_{0.3}Zn_{0.7}O_{1.3}$/Si junctions which are fabricated by two interface formation processes, and qualitatively analyzing the band-to-band tunnelling (BTBT) current and trap-assisted tunnelling (TAT) current components.

2. Experimental Procedure

Fig. 1 shows a schematic diagram of the prepared sample. $Ti_{0.3}Zn_{0.7}O_{1.3}$ films with an initial (a) TiO_2 layer or (b) ZnO layer in a 3:7 ratio of TiO_2/ZnO multiple stacked structure on p-Si substrates (carrer concentration: ~10^{19} cm^{-3}) were deposited by laser ablation (PLD) with a KrF excimer laser (λ=248 nm). Here, each single layer is consisted of less than mono-atomic layer and each fabrication method is referred to as (a) TiO_2 first and (b) ZnO first. The total film thickness was set to 5 nm, respectively. Other conditions were oxygen pressure of 10^{-4} Torr and substrate temperature of 300 °C. For electrical measurement, Al top electrodes with a diameter of 100 μm were formed by vacuum evaporation using a metal mask and Ti/Pt back electrodes were formed by DC sputtering overall. Finally, forming gas annealing treatment (4% H_2: N_2 atmosphere) at 400 °C for 30 min was carried out.

The temperature dependence of electrical properties was evaluated using I-V measurements with a cryostat at temperatures ranging from 60 K to 300 K, with a voltage step of 20 mV.

3. Results and Discussion

First, we evaluated the temperature dependence of the I-V characteristics of the both samples. As a result, a rise in current was confirmed even when a reverse bias was applied regardless of the fabrication process or temperature. Therefore, we analyzed the electric field dependence of the BTBT current in the reverse bias region, and that existence was observed shown in Fig.2. In addition, the BTBT barrier was lower in the TiO_2 first from the slope of the graph were confirmed. Furthermore, the electric field dependence of the TAT current was analyzed and that existence was also observed. This indicates the presence of tail states that contribute to electron traps in the interfacial SiO_2 layer or oxide semiconductor and at the interface. To quantitatively evaluate the depth of this trap level, the arrhenius plot analysis was performed, as shown in Fig. 3 [5]. We found that the activation energy of TiO_2 first was significantly lower than that of ZnO first in this study and the ZnSnO TFET in previous study [3]. The reduction in the BTBT barrier and activation energy in TiO_2 first can be explained by the difference in interfacial properties. We have already revealed that TiO_2 first prevents the formation of metal silicate microcrystallites and forms an interface layer with low roughness than ZnO first

by the effects of high oxygen bond dissociation energy of Ti, and this is thought to suppress deep trap states in the interface and oxide semiconductor layer [4].

4. Conclusions

To investigate the relationship between the interface formation process and the tunneling current characteristics, we evaluated the temperature and electric field dependence of the tunneling current components in two types of $Ti_{0.3}Zn_{0.7}O_{1.3}$/Si junctions with defferent fabrication processes. As a result, we found that TiO_2 first/Si, which has an interface layer with less microcrystal formation and low roughness, has the smaller BTBT barrier and activation energy, and can suppress electron trapping at the interface. This result suggests that the increase in on-current of TFETs and the reduction of S.S. can be realized by optimizing the interface formation process and suppressing trap states in the interface and oxide semiconductor layer.

Acknowledgements

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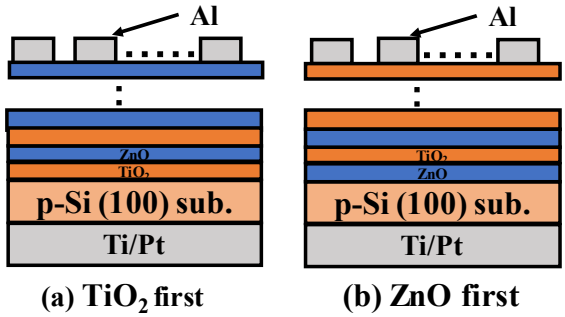

Fig. 1 Schematic diagram of $Ti_{0.3}Zn_{0.7}O_{1.3}$/Si sample structures for (a) TiO_2 first, and (b) ZnO first.

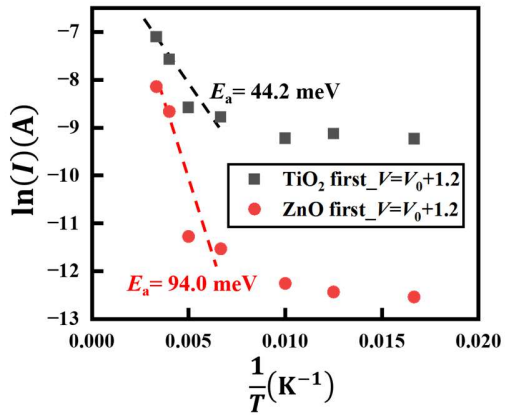

Fig. 3 Arrhenius plots of TiO_2 first and ZnO first/Si.

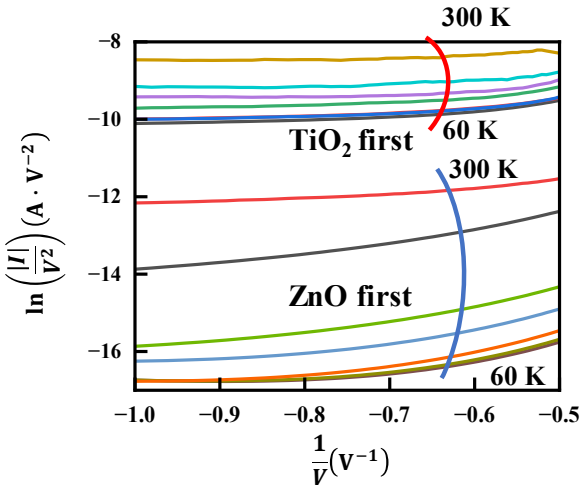

Fig. 2 Electric field dependence of the BTBT current with TiO_2 first and ZnO first/Si.

Classical Molecular Dynamics Simulation of Ferroelectric Properties of a-HfO_2

Jumpei Ohba, Sora Yamamoto, Yusuke Nishimura,Takanobu Watanabe
Faculty of Science and Engineering, Waseda University,
3-4-1 Okubo, Shinjuku, Tokyo 169-8555 Japan
Email:junpeita@akane.waseda.jp / Phone: +81-90-9376-9358

1. Introduction

HfO_2 thin films have been reported to exhibit ferroelectricity even at film thicknesses of several nanometers [1,2] and are attracting attention as next-generation nonvolatile memory materials. The origin of the ferroelectric property of HfO_2 film is attributed to the $Pca2_1$ phase [3], but there are still many unresolved issues, such as the mechanisms by which residual polarization depends on impurity doping and rapid thermal treatment. Several authors reported molecular simulation studies on the ferroelectricity of HfO_2 crystals [4] by using first-principles molecular dynamics (MD) and on the structural phase transition of HfO_2 [6] by using a machine learning MD (DeepMD) [5]. However, no MD simulation has been reported that reproduces the ferroelectricity of HfO_2 at sizes of several nanometers or larger, which are close to real thin films.

In this study, we performed classical MD calculations of HfO_2 applying an external electric field. We employed the Born-Mayer-Huggins (BMH) potential [7-10], which is one of simplest interatomic interaction models representing ionic bonding. Significant hysteresis has been reproduced in an amorphous HfO_2 (a-HfO_2) model.

2. Experimental Procedure

Fig. 1 shows the model used in the MD simulation: (a) bulk a-HfO_2, (b) bulk a-SiO, and (c) a-SiO_2/a-HfO_2/a-SiO_2 interface structures. Three-dimensional periodic boundary condition is posed for all models. These amorphous structures were generated by melting the crystalline HfO_2 and SiO_2 structures through three processes: melting at 8000 K, isothermal isobaric treatment at 1200 K, and cooling to 300 K. An electric field was applied along the z-axis (see Fig.1), and dipole moment component along z-axis was calculated. The external electric field was increased by +0.05 MV/cm every 0.3 ps until to reach +20 MV/cm. Then, it was swept back to -20 MV/cm at the same rate. Finnally, it was again increased again at the same rate to +20 MV/cm. The parameter set of the potential was determined by refitting the Morse-BKS potential for the Hf,Si,O system [10] with the BMH potential. The potential formula the parameters at that time are shown in Table I.

3. Results and Discussion

Fig. 2 shows the electric field–polarization characteristics of a-HfO_2, a-SiO_2, and a-SiO_2/a-HfO_2/a-SiO_2 interface structures. A clear hysteresis is reproduced in the a-HfO_2 model. The difference between maximum and minimum residual polarization was $Pr^+ - Pr^- = 24\ \mu C/cm^2$. The polarization was calculated by the displacement of each ion from its initial position. Figure 3 shows the displacement of oxygen ions when an electric field is applied. The O ions predominantly undergo plastic deformation in the opposite direction to the applied electric field. Figure 4 shows the displacement for each element as a function of original z-position. It can be seen that the contribution of O ion movement is overwhelmingly greater than Hf.

The a-SiO_2/a-HfO_2/a-SiO_2 layered model also exhibits a smaller hysteresis of approximately $Pr+ - Pr- \approx 4\ \mu C/cm^2$. The reduction in the ferroelectric hysteresis is considered to be the depolarization due to polarized charges appeared at a-HfO_2/a-SiO_2 interfaces. Fig. 5 shows the charge distribution and internal electric field distribution along z-axis when an electric field of ±20 MV/cm is applied. The positive and negative charges in the dipole layers at both interfaces are asymmetrical, and their relative magnitudes are reversed between the +20 MV/cm and -20 MV/cm. This can be interpreted as the induced polarization charges being superimposed on the dipoles at a-HfO_2/a-SiO_2 interfaces. The altered charge distribution within the interface dipole layer generates an electric field within the HfO_2 layer opposite to the external electric field, thereby weakening the ferroelectric hysteresis of the a-HfO_2 layer as a ferroelectric material.

4. Conclusions

We demonstrated that the ferroelectricity of a-HfO_2 film can be simulated in large scale by means of classical molecular dynamics employing a very simple, pairwise interaction for ionic materials. Origin of the ferroelectricity has been confirmed as the plastic deformation of O ions upon the external electric field application. In the a-SiO_2/a-HfO_2/a-SiO_2 layered structure, the polarization charge appears at the interfaces, thereby the charge distribution in the interface dipole layer altered. Since the employed BMH potential can handle various kinds of metal cations simultaneously, our approach is considered effective for studying the effects of heterogeneous interfaces and impurities in ferroelectric HfO_2 films.

Acknowledgements
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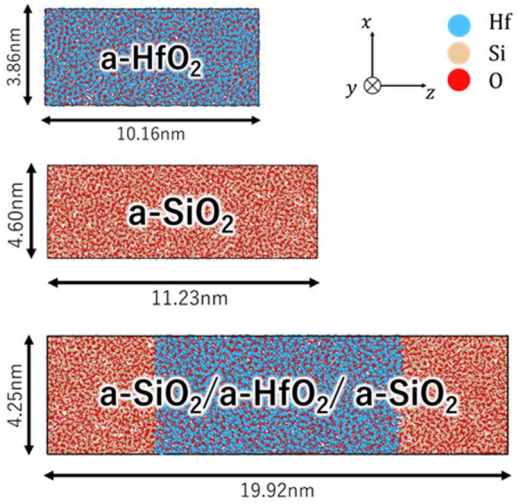

Fig.1 Simulation models.

Table I Parameters for the BMH potential. A pair energy between atoms i and j is defined as $V_{ij} = \frac{q_i q_j e^2}{4\pi\varepsilon_0 r_{ij}} + A_{ij}\exp\left(\frac{\sigma_{ij}-r_{ij}}{\rho_{ij}}\right) - \frac{C_{ij}}{r_{ij}^6} + \frac{D_{ij}}{r_{ij}^8}$.

i	j	q_i (e)	q_j (e)	A_{ij} (eV)	σ_{ij} (Å)	ρ_{ij} (Å)	C_{ij} $(eV*$ Å$^6)$	D_{ij} $(eV*$ Å$^8)$
Hf	Hf	2.4	2.4	0.0	0.0	1.0	0.0	0.0
Hf	O	2.4	-1.2	23500.0	0.0	0.205	15.0	-84.0
O	O	-1.2	-1.2	1388.769	0.0	0.3584364	175.0027	999.99938
Si	Si	2.4	2.4	0.0	0.0	1.0	0.0	0.0
Si	O	2.4	-1.2	17074.53	0.0	0.2021379	132.0058	39.0
Hf	Si	2.4	2.4	0.0	0.0	1.0	0.0	0.0

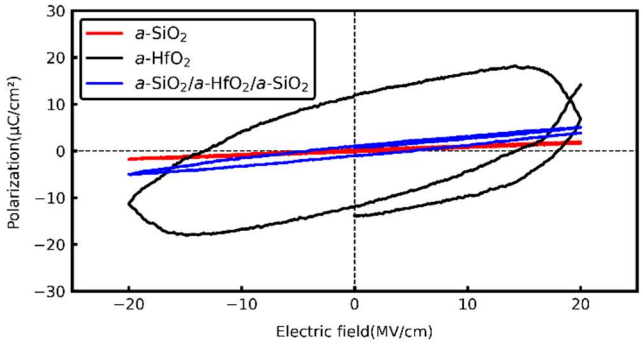

Fig.2 Polarization vs. electric field plots.

Table II Pr^+–Pr^- values.

Model	Pr^+–Pr^-(μC/cm²)
(a) a-HfO_2	23.969
(b) a-SiO_2	0.325
(c) a-SiO_2/a-HfO_2/a-SiO_2	2.157

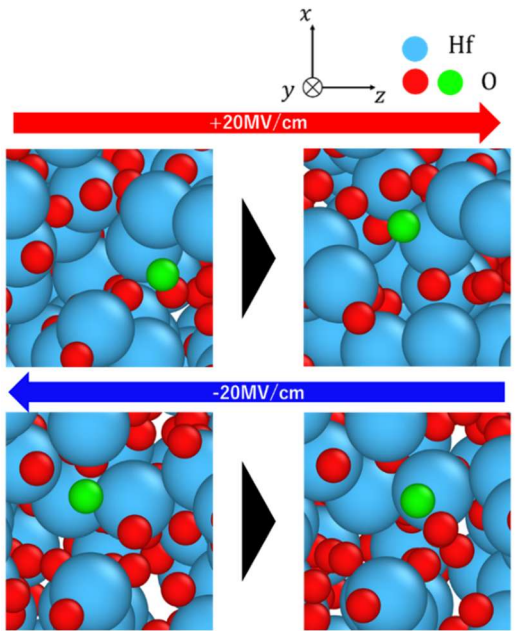

Fig.3 Displacement of oxygen ions in a-HfO_2 when an electric field is applied.

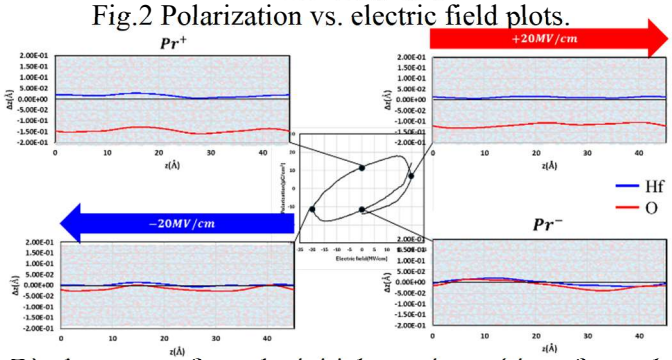

Fig.4 Displacements from the initial atomic positions for each element in a-HfO_2 under an applied electric field.

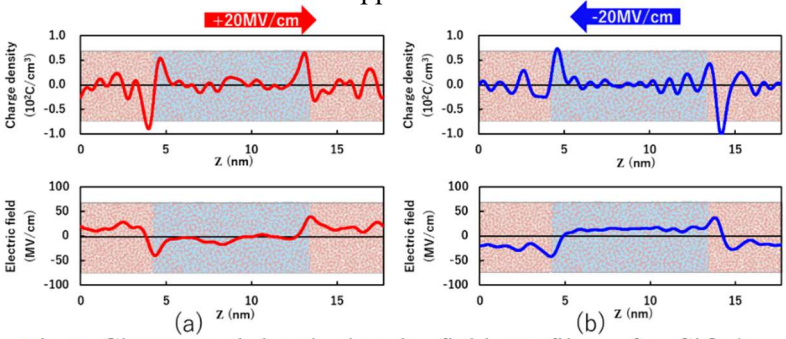

Fig.5 Charge and local electric field profiles of a-SiO_2/a-HfO_2/a-SiO_2 under external fields of (a) +20MV/cm (b) -20MV/cm.

Effects of Al Concentration and Annealing Method on Crystalline and Ferroelectric properties of Al:HfO_2 Thin Films

Tomoya Mifune[1], Hideaki Tanimura[1,2], Yuma Ueno[2], Yusuke Tani[2], Yukiya Sano[1], Hironori Fujisawa[1], Seiji Nakashima[1], Ai I. Osaka[1], Shinichi Kato[2] and Takumi Mikawa[2]
[1]Univ of Hyogo, [2] SCREEN Semiconductor Solutions
[1]Shosha 2167, Himeji, Hyogo 671-2280, Japan, [2]Takamiya-cho 480-1, Hikone, Shiga 522-0292, Japan
Email: ei24i023@guh.u-hyogo.ac.jp / Phone: +81-79-267-4883

1. Introduction

HfO_2-based ferroelectrics have attracted considerable attention as promising candidates for next-generation non-volatile devices owing to their excellent scalability and high compatibility with CMOS processes. Among them, Al-doped HfO_2 (HAO) exhibits high thermal stability, making it suitable for high-temperature processes, such as 3D-NAND fabrication [1]. However, HAO thin films typically require high crystallization temperatures, and conventional rapid thermal annealing (RTA) can potentially cause damage to underlying devices. To address this issue, we focused on flash lamp annealing (FLA), which enables millisecond-scale crystallization with a reduced thermal budget. Our previous work demonstrated that FLA-crystallized HAO films exhibit polarization values approximetly 1.6 times higher than those crystallized through RTA [2]. Nevertheless, the influence of Al concentration on the crystallinity and ferroelectric properties of FLA-crystallized HAO films remains insufficiently explored. In this study, we fabricated HAO thin films with Al concentrations ranging from 0 to 12 at% and systematically evaluated their crystallinity and ferroelectric properties, comparing the effects of different annealing processes.

2. Experimental Procedure

TiN/HAO/TiN capacitors were fabricated on Si substrates. HAO thin films with a thickness of 10 nm were deposited by atomic layer deposition (ALD), with the Al composition ratio, Al/(Al+Hf), controlled between 0 and 12 at%. Different annealing processes were employed for crystallization: (i) FLA with a preheating temperature of 400 °C and a peak temperature of 1000 °C for 5 ms in N_2 atmosphere; (ii) RTA at 600 °C for 1 min in N_2 atmosphere. The crystallinity of the films was evaluated by grazing-incidence X-ray diffraction (GIXRD), and ferroelectric properties were characterized by polarization-electric field (*P–E*) hysteresis measurements.

3. Results and Discussion

Figure 1 shows the XRD patterns of HAO films after FLA and RTA. Crystallization was observed up to 6 at% Al for RTA and up to 9 at% Al for FLA. In both processes, the peak intensity was maximized around 2-3 at% Al, indicating that this concentration range is optimal for crystallization regardless of the annealing method. Furthermore, FLA yielded higher peak intensities than RTA, suggesting improved crystallinity. Figiure 2 shows the dependence of the diffraction angle on Al concentration. As the Al content increased, the peaks shifted toward higher angles, indicating that tensile stress was induced in the film due to the substitution of smaller Al ions for Hf. FLA-crystallized films exhibited peaks at higher angles than RTA-treated films, implying that stronger tensile stress was introduced. Since tensile stress promotes the formation of the ferroelectric orthorhombic (o) phase [3], FLA is considered more effective than RTA in facilitating o-phase formation. Figiure 3 presents the P–E hysteresis loops of HAO films with varying Al concentrations. FLA-crystallized films exhibited higher polarization values than RTA-treated films, with the most significant improvement (approximately 1.4 times) observed at 2 at% Al. Taken together with the XRD results, these findings suggest that the enhanced polarization in FLA-treated films originates from the stronger tensile stress, which increases the fraction of the o-phase.

4. Conclusions

Both FLA and RTA processes yielded maximum crystallinity and ferroelectricity at an Al concentration of 2 at%. FLA introduced greater tensile stress than RTA, promoting o-phase formation and enhancing polarization properties. These results demonstrate that FLA not only enables low-thermal-budget crystallization but also effectively induces tensile stress in HAO thin films, thereby improves ferroelectric performance.

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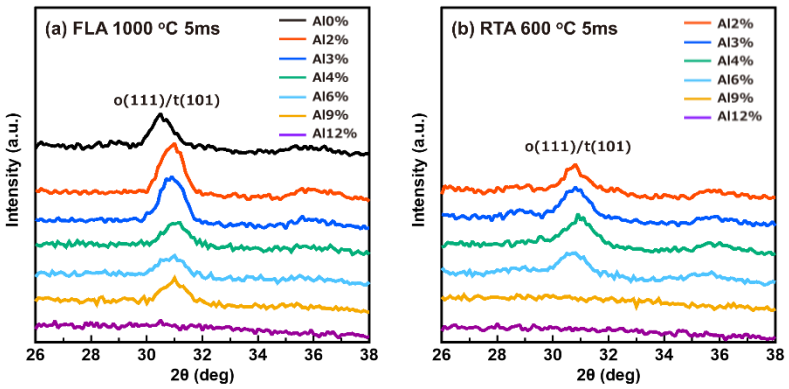

Fig. 1 Al concentration dependence of XRD patterns. HAO films crystallized by (a) FLA and (b) RTA exhibited the highest peak intensity around 2-3 at% Al. FLA can crystallized HAO films up to 9 at% Al.

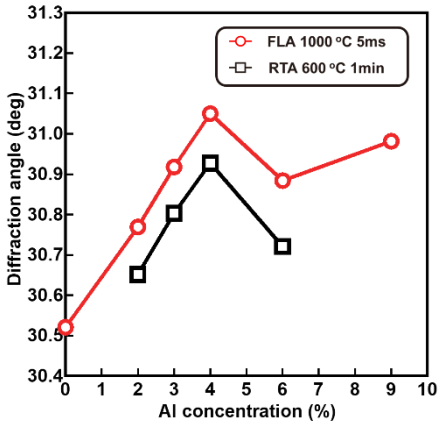

Fig. 2 Al concentration dependence of HAO diffraction angles. The diffraction angles shifted toward higher angles with increasing Al concentration, suggesting tensile stress.

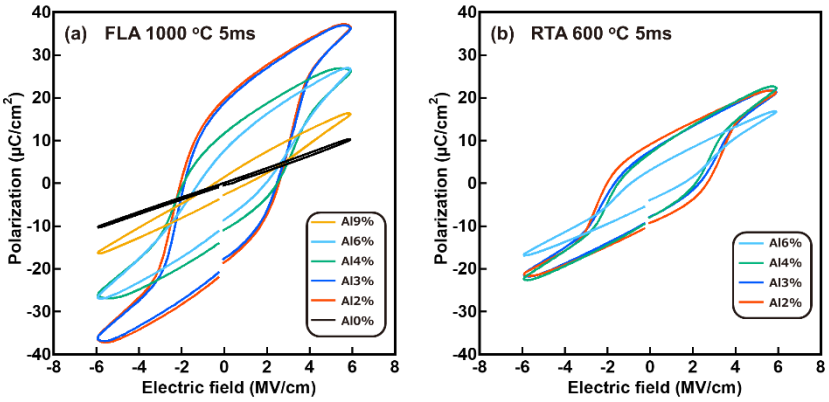

Fig. 3 *P*–*E* hysteresis loops of HAO films with varying Al concentrations. (a) FLA- and (b) RTA-crystallized films showed the highest polarization at 2 at% Al with $2P_r$ = 37.9 and 26.3 μC/cm², respectively.

Consideration on the Coexisting Positive- and Negative-Imprinted Ferroelectric Domains and Their Imprint-Recovery in Non-Doped HfO_2 MFM Capacitors

Yukinori Morita, Shutaro Asanuma, Hiroyuki Ota, and Shinji Migita
SFRC, AIST
Tsukuba, Ibaraki 305-8569, Japan
Email: y.morita@aist.go.jp / Phone: +81-80-2216-4272

1. Introduction

The HfO_2-based ferroelectrics (Fe-HfO_2) have attracted attention and are being studied for their potential application in memory devices. One of the challenges in memory applications is the instability of polarization (wake-up and fatigue) caused by the application of cyclic voltages. This is thought to be caused by changes in the distribution of oxygen vacancies in the Fe-HfO_2 film due to the cyclic electric field. Changes in the distribution of charged vacancies and interstitial oxygen are also causes of unbalanced polarization characteristics, known as imprint. These issues need to be understood and addressed.

We found that the ferroelectric non-doped HfO_2 prepared by changing the annealing conditions exhibited a polarization-voltage (PV) shape different from that of normal ferroelectric properties. Evaluating the change in the PV shape when applying a cyclic voltage to these samples, it was suggested that the initial imprinted state of ferroelectric domains may be recovered by applying a cyclic voltage.

2. Experimental Procedure

Metal-ferroelectric-metal (MFM) capacitors were prepared with non-doped HfO_2 [1-3]. In the fabrication process, a Si wafer was first cleaned with diluted HF, and a 10-nm-thick bottom TaN electrode was deposited using DC sputtering. A 10-nm-thick HfO_2 layer was then deposited by RF sputtering using a HfO_2 target. A 10-nm-thick TaN top electrode was also deposited by DC sputtering. Crystallization annealing was subsequently performed at temperatures ranging from 465 to 992 °C using the rapid thermal annealing (RTA) method in a vacuum. Finally, top and bottom Al electrodes were fabricated by photolithography and dry etching.

3. Results and Discussion

Figure 1 shows the PV characteristics of the HfO_2 MFM capacitors with varying annealing temperature. By annealing at 780°C, the HfO_2 capacitor exhibits ferroelectricity as shown in (a). With increasing the annealing temperature, in Fig. 1(b), the PV shape slightly changes to a polygonal-like shape, which may reflect responses in multiple domains. In Figure 1(c), the shape changes further to a polygonal-like shape, which looks like a triple state with an intermediate polarization state added. Figure 2 shows the change in the PV shape with a ±3V triangular pulse applied for 100 cycles to the MFM capacitors shown in Figure 1. In Figure 2(a), a noticeable shift in the lower part of the PV curve is observed due to the voltage cycle increase. Also, in Figures 2(b) and (c), the direction of the characteristic shift due to voltage cycle application is opposite between the upper and lower parts of the PV curve, which is indicated by red arrows in the figure. After these characteristic shape changes, in (b) and (c), the PV shape approaches the shape of the normal PV curve corresponding to bistable states from the polygonal-like PV mentioned in Figure 1. Figure 3 shows a model of the phenomenon in which the PV shape returns from a polygonal-like to a normal shape. We assume that a polygonal-like PV appears due to two types of domains that are previously imprinted in opposite directions by thermal annealing. The imprint is recovered by applying a voltage cycle, as shown in Fig. 3(b), causing a transition from a polygonal-like to a normal PV, which can explain the phenomenon well.

Acknowledgements

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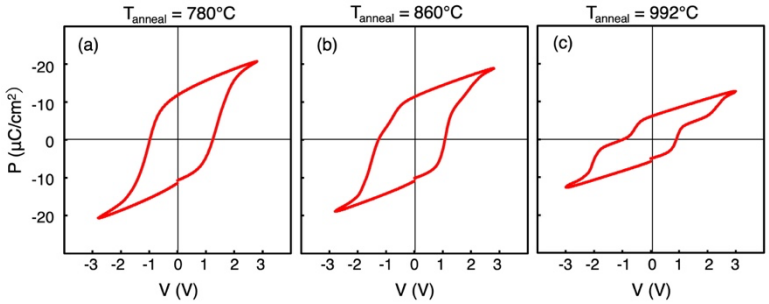

Fig. 1 PV characteristics of MFM capacitors with non-doped HfO_2. Annealing temperatures of the MFM capacitors are (a) 780, (b) 860 and (c) 992°C, respectively.

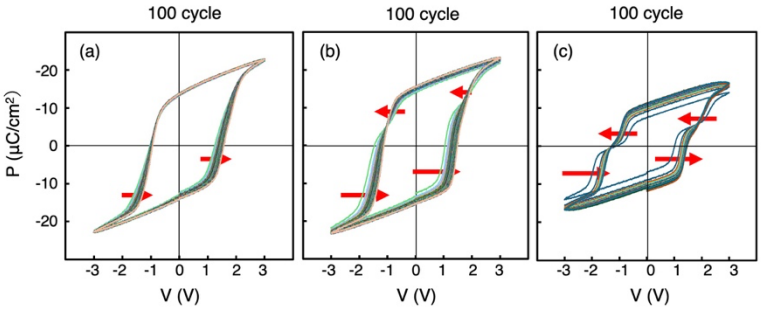

Fig. 2 Overlayed PV characteristics of MFM capacitors of non-doped HfO_2 with 100-cycle triangular pulse application. Red arrows indicate shift direction of the curves from 1st to 100th voltage cycles. Annealing temperatures of the MFM capacitors are (a) 780, (b) 860 and (c) 992°C, respectively.

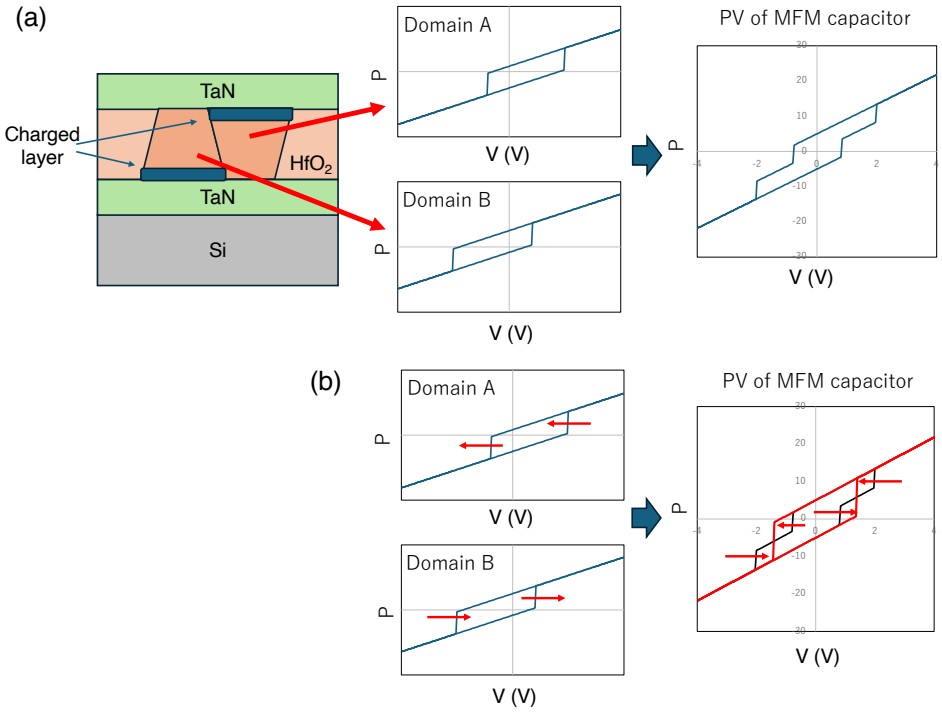

Fig. 3 Possible model of polygonal-like PV and return of the PV shape after cyclic voltage apply. (a) Schematic model of MFM capacitor cross-section and PVs of initially imprinted domains. Sum of these PVs shows polygonal-like PV as shown in Fig. 1(c). (b) Imprint recovery in initially imprinted domains by application of voltage cycles implies shift of individual PVs. As a result, polygonal-like PV changes to normal shape.

Polarization Inversion in Hf-based Oxide Layer with High Si Content in MOS Structure

Riku Kayagi[1], Wataru Yasuda[2], Akio Ohta[3], Katsunori Makihara[2],
Yusuke Ichino[1], Yoshiyuki Seike[1], Tatsuo Mori[1], and Noriyuki Taoka[1]
[1]Aichi Inst. Tech., [2]Nagoya Univ., [3]Fukuoka Univ.
[1]1247 Yachigusa, Yakusa-cho, Toyota, 470-0392, Japan
Email: v25707vv@aitech.ac.jp, ntaoka@aitech.ac.jp / Phone: +81-565-48-8121

1. Introduction

Ferroelectric properties have been demonstrated in orthorhombic Hf-based oxide films with nanometer-scale thicknesses, achieved through precise control of the crystal structure[1]. Due to this ferroelectricity, orthorhombic Hf-based oxides have attracted significant attention as promising gate dielectric materials for steep-slope devices that can improve the subthreshold characteristics of MOSFETs. These ferroelectric Hf-based oxide layers exhibit a remanent polarization ~20 μC/cm^2 with a Si doping concentration of ~1%[2]. However, this value corresponds to a charge density of ~10^{14} cm^{-2}, which is far larger than the carrier density modulated by gate voltage in a typical MOSFET. Therefore, precise control of remanent polarization as well as the MOS interface quality is crucial for realizing steep-slope devices utilizing Hf-based oxide layers.

In this study, MOS capacitors with Hf-based oxide layers were fabricated by post-oxidation of Hf layers with different initial thicknesses. The correlation between the initial Hf layer thickness and the electrical properties of the MOS capacitors was systematically investigated.

2. Experimental Procedure

As shown in Fig. 1, an n$^+$-Si(100) substrate with a resistivity of ≤0.005 Ω·cm was cleaned using a conventional wet cleaning process. A 2.5-nm-thick SiO_2 interfacial layer was then formed by atomic layer deposition (ALD) with bis(diethylamino)silane and oxygen plasma. Subsequently, Hf films with thicknesses (t_{Hf}) ranging from 1 to 4 nm were deposited by electron-beam evaporation and thermally oxidized in an oxygen ambient at 600–900 °C for 10 min using a lamp annealing system, resulting in the formation of Hf-based oxide layers. Finally, MOS capacitors were fabricated with Ni top electrodes and Al bottom electrodes. X-ray photoelectron spectroscopy (XPS) was performed after the oxidation. Their *C*-*V* characteristics and charge response under pulse bias were systematically evaluated.

3. Results and Discussion

To clarify the chemical bonding features after the oxidation, the XPS measurements were carried out. In the Hf 4f spectra of the sample with t_{Hf} = 2 nm (Fig. 2(a)), the peaks observed at the binding energies of 19 and 21 eV show higher intensities for the oxidation at 900°C compared with those for 600°C and the as-deposited sample. Similarly, in the Si 2p spectra (Fig. 2(b)), the intensity near 103 eV is markedly enhanced at 900 °C. These results indicate the formation of Hf-silicate, which originates from Si diffusion from the Si substrate into the Hf layer. Angle-resolved XPS (Fig. 3) revealed a significant increase in Si content within the Hf-based oxide layer. After oxidation at 900 °C, the Si concentration exceeded 10%, and reached 16% at a take-off angle (TA) of 15°, suggesting that Si atoms diffuse toward the oxide surface despite the presence of the ALD-SiO_2 interlayer.

The diffusion of Si strongly affects the electrical properties of the Hf-silicate layer. Figure 4 shows the *C*-*V* curves measured at 1 MHz for t_{Hf} = 1, 2, and 4 nm after the oxidation at 900 °C. The capacitance under strong accumulation bias condition decreases with increasing t_{Hf}. From the capacitance equivalent thickness (CET) and the estimated physical thickness of HfO_2, the relative permittivity was found to be ~12 (Fig. 5), which is smaller than that of ferroelectric HfO_2. This is consistent with the Hf-silicate formation. In addition, clear hysteresis loops were observed in the *C*-*V* curves for all t_{Hf} values (Fig. 4). If the Hf-silicate exhibits ferroelectricity, these loops can be attributed to polarization inversion. However, *C*-*V* measurements are generally influenced by slow traps, making quantitative evaluation difficult.

To minimize the effect of slow traps, charge responses to pulse bias (V_{pls}) were examined using a Sawyer–Tower circuit with a 1 kHz triangular pulse (Fig. 6, inset). The stored charge Q_{ref} was obtained from $C_{ref} \times V_{ref}$, where C_{ref} is the reference capacitance. Since C_{ref} is constant, the measured Q_{ref} reflects the capacitance of the MOS capacitors. While devices with t_{Hf} = 1 and 4 nm oxidized at 900 °C showed no hysteresis, those with t_{Hf} = 2 nm oxidized at 750 °C and 900 °C clearly exhibited hysteresis loops (Fig. 6). The change in Q_{ref} at V_{pls} = 0

was smaller than previously reported values [2]. These findings suggest that the polarization inversion can be modulated by controlling Si diffusion and subsequent Hf-silicate formation.

4. Conclusions

The Hf-based oxide layers were successfully formed by post-oxidation of the Hf layers on ALD-SiO_2. XPS analysis revealed a high Si content in the oxide layers, indicating the formation of Hf-silicate. Furthermore, the MOS capacitors with the Hf-silicate layers exhibited hysteresis loops in both the *C-V* and *Q–V* characteristics for the case of t_{Hf} = 2 nm oxidized at 750 °C and 900 °C. Although the change in Q_{ref} was relatively small, its controllability was confirmed. These findings provide valuable insights toward the realization of the steep-slope devices.

Acknowledgements

We would like to express our sincere gratitude to Professor Seiichi Miyazaki for their valuable advice and the fruitful discussions. Also, we would like to thank K. Sako and N. Takasu for measurement and discussion.

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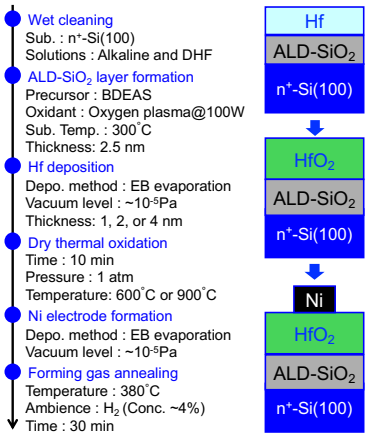

Fig. 1: Process flow of the MOS capacitors and schematic diagrams of the related structures.

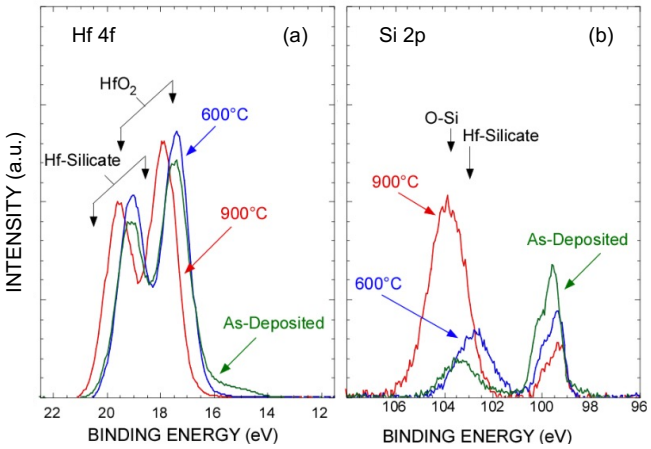

Fig. 2: XPS spectra of (a) Hf 4f and (b) Si 2p. Here, intensities of the spectra were normalized by integrated intensity of Hf 4f spectrum, and binding energies were corrected using binding energy of C-H bonding in C1s spectra.

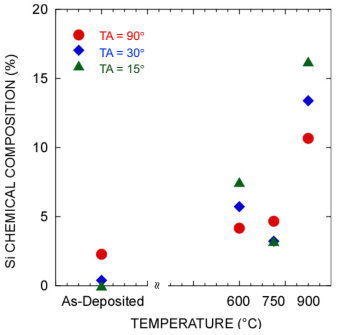

Fig. 3: Si composions evaluated from the Si 2p XPS spectra.

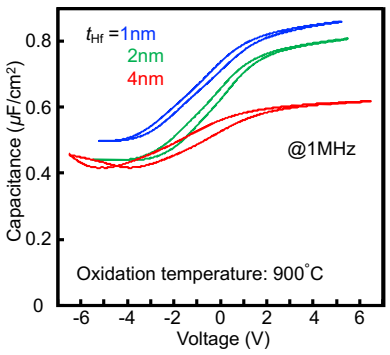

Fig. 4: *C-V* curves of the MOS capacitor with the different t_{Hf}. Here, the Hf-based oxide layers were formed by the oxidation at 900°C.

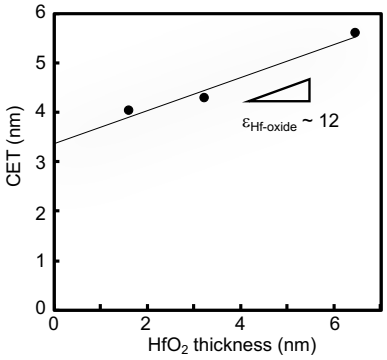

Fig. 5: CET vs HfO_2 thickness plot.

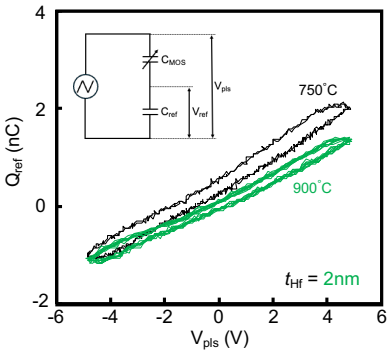

Fig. 6: Q_{ref} *-V* curves evaluated from Sawyer-Tower circuit with 1kHz triangular pulse.

Effect of Plasma Treatment on Performance of AlScN-Based Ferroelectric Tunnel Junctions

Yuki Yamada[1], Kazuki Goshima[1], Yoshiharu Kirihara[1], Ryoichi Kawai[1],
Kuniyuki Kakushima[2], Hiroshi Nohira[1] and Yuichiro Mitani[1]
[1]Tokyo City University, 1-28-1 Tamazutsumi, Setagaya-ku, Tokyo 158-8557, Japan,
[2]Institute of Science Tokyo, 4259 Nagatsuta-cho, Midori-ku, Kanagawa 226-8503, Japan
Email: g2481285@tcu.ac.jp / Phone: 03-5707-0104

1. Introduction

Recent advances in artificial intelligence (AI) and machine learning have increased the demand for high-speed, low-power processing technologies. Computing-in-memory (CiM) devices based on aluminum scandium nitride (AlScN) ferroelectric tunnel junctions (FTJ) offer integrated memory and computation in a cross-point structure, enabling in-situ multiply–accumulate operations for efficient parallel computing [1,2]. However, the reduction of the voltage for polarization switching still poses as a significant challenge for practical use. While thinning the film effectively lowers the polarization switching voltage, it also increases leakage current and tends to degrade the I_{on}/I_{off} ratio. Previous studies have reported that plasma nitridation and plasma oxidation treatments can suppress leakage current in AlScN films and improve the I_{on}/I_{off} ratio [3,4]. The objective of this study is to reduce the switching voltage while maintaining a high Ion/Ioff ratio by combining the plasma treatment with film thinning of the ferroelectric AlScN.

2. Experimental Procedure

FTJ devices using AlScN were fabricated based on the process flow shown in Fig. 1. First, a 10 nm thick TiN bottom electrode was deposited on an n^+-Si substrate using RF sputtering. Then, AlScN thin films with 30% scandium concentration were deposited by DC sputtering at a substrate temperature of 400 °C, with an Ar:N_2 gas flow ratio of 5:10. The film thicknesses were set to 20 nm, 35 nm and 50 nm. After AlScN deposition, some samples were subjected to plasma nitridation and plasma oxidation for 1 minute each (hereafter referred to as “plasma treatment”). Subsequently, an Al top electrode was deposited on the TiN layer by RF sputtering, followed by photolithography and dry etching to pattern the electrodes. Finally, Al was deposited on the backside of the substrate to form a back contact, completing the two-terminal FTJ memory cell structure.

3. Results and Discussion

Figure 2 shows the typical capacitance–voltage (C–V) characteristics with and without plasma treatment, while Figure 3 presents the relationship between film thickness and coercive voltage. As film thickness decreases, the capacitance peak shifts towards lower voltages, indicating that film thinning is effective for a reduction in operation voltage. It has been demonstrated that, as a result of plasma treatment, the capacitances decrease and the coercive voltages increase for each film thickness of AlScN.

Figure 4 shows the current density-voltage (J–V) characteristics. As film thickness decreases, the leakage current increases and the I_{on}/I_{off} ratio decreases, as shown in Fig. 4(a). However, the leakage current can be improved by plasma treatment as shown in Fig. 4(b). Figure 5 shows the I_{on}/I_{off} ratio at 5V for the different AlScN thickness. In the absence of plasma treatment, the I_{on}/I_{off} ratio decreases monotonously as the thickness of the AlScN film is reduced. On the other hand, in the case with plasma treatment, the I_{on}/I_{off} ratio increases regardless of the AlScN thickness. Especially, the plasma-treated sample with 35 nm AlScN exhibits the higher I_{on}/I_{off} ratio. These results suggest that the optimum plasma treatment condition depends on the film thickness. The plasma nitridation reduces nitrogen vacancies in the AlScN film, thereby suppressing leakage current. Concurrently, the plasma oxidation forms an interfacial oxide layer, thereby enhancing the I_{on}/I_{off} ratio [3,4]. That is, in the case of the 50nm AlScN film, the plasma treatment is insufficient, and consequently the modified region could be small as shown in Fig. 6(a). In contrast, in the case of 20nm AlScN film, the excessive nitrogen incorporation likely inhibits polarization switching, leading to a decreased I_{on}/I_{off} ratio. These interpretations are consistent with angle-resolved hard X-ray photoelectron spectroscopy (AR-HAXPES) results, showing that 1 min plasma nitridation/oxidation treatments influence the AlScN film up to ~20 nm from the surface [5].

4. Conclusions

In this study, we investigated the effects of plasma nitridation/oxidation treatments with film thinning on the performance of AlScN FTJ devices. As a result, for thinner AlScN FTJ devices, the optimal plasma treatment conditions depending on film thickness are crucial for realizing high-performance FTJ devices.

Acknowledgements

We would like to thank Mr. Arimitsu Kato (Institute of Science Tokyo) for his great help in carrying out this research.

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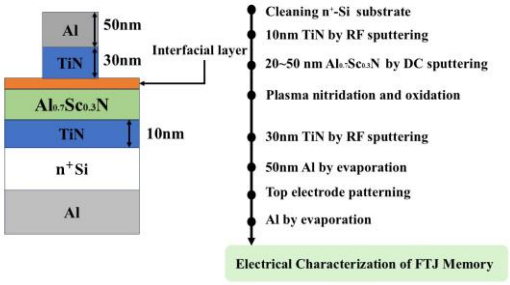

Fig. 1 AlScN FTJ memory structure used in this work

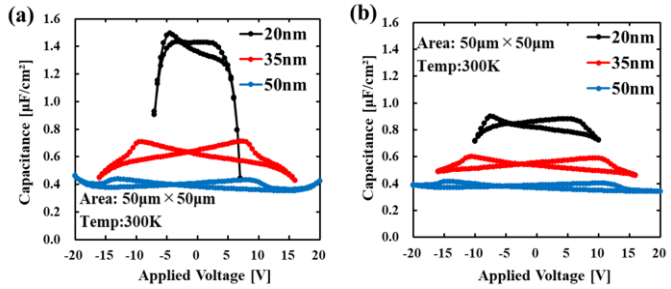

Fig. 2 Capacitance–voltage (C–V) characteristics of AlScN-based FTJ devices: (a) as-deposited, (b) plasma nitridation (60 s) + plasma oxidation (60 s).

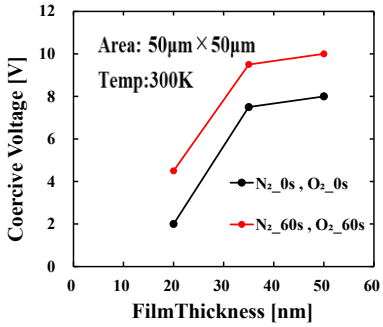

Fig. 3 Relationship between thickness and coercive voltage.

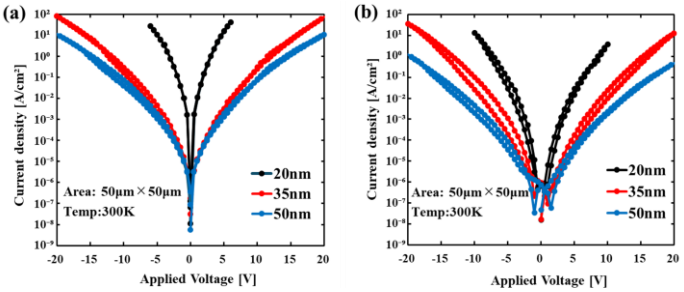

Fig. 4 The current density-voltage (J–V) characteristics of AlScN-based FTJ devices: (a) as-deposited, (b) plasma nitridation (60 s) + plasma oxidation (60 s).

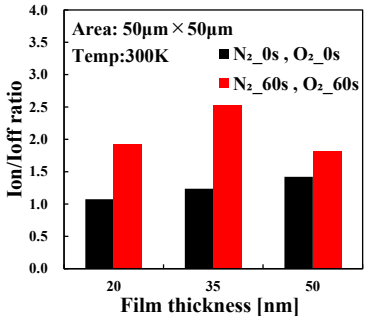

Fig. 5 The I_{on}/I_{off} ratio at 5V for each film thickness.

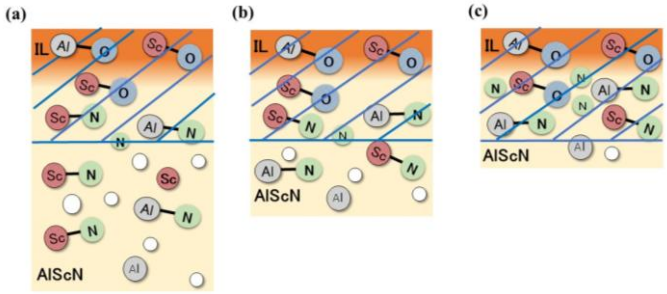

Fig. 6 Schematic illustration of AlScN films after nitridation and oxidation treatment: (a) 50 nm, (b) 35 nm, (c) 20 nm.

Study on Defect Generation in Ferroelectric AlScN from TDDB Statistical Point of View

Haruro Inoue[1], Yuki Yamada[1], Kazuki Goshima[1], Yoshiharu Kirihara[1], Kuniyuki Kakushima[2], Hiroshi Nohira[1] and Yuichiro Mitani[1]
[1]Tokyo City University, 1-28-1 Tamazutsumi, Setagaya-ku, Tokyo 158-8557, Japan,
[2]Institute of Science Tokyo, 4259 Nagatsuta-cho, Midori-ku, Kanagawa 226-8503, Japan
Email: g2481216@tcu.ac.jp / Phone: +81-3-5707-0104

1. Introduction

The Weibull distribution of the time-dependent dielectric breakdown (TDDB) for dielectric thin films is significant not only for the long-term reliability, but also it provides many insights related to the defect in the thin films. For instance, the defect size can be discussed from the Weibull slope (β) [1]. In this work, we focus on the Weibull distribution of the AlScN Metal-Ferroerectric-Metal (MFM) devices. Ferroelectric AlScN has attracted much attention for next-generation electron devices, including non-volatile memory applications, owing to their large remanent polarization, stable crystal structure, and compatibility with CMOS processes [2, 3]. This paper discusses defect generation in AlScN films through an analysis of the experimental results of TDDB characteristics.

2. Experimental Procedure

The process flow of the AlScN-MFM device is shown in Fig. 1. First, 10 nm of TiN was deposited on an n^+-Si substrate by RF sputtering. Next, 50 nm of AlScN with a Sc concentration of 30% was deposited by DC sputtering at 400 °C with an Ar:N_2 gas ratio of 5:10, followed by plasma oxidation for 1 minute. Subsequently, TiN and Al were deposited as the top electrodes. The electrode pattern was defined by photolithography, and the top electrode was processed by dry etching. Finally, Al was deposited on the backside of the n^+-Si substrate to form a back contact, completing the two-terminal MFM structure. Similarly, AlScN-MFMs with a Sc concentration of 20% were also fabricated.

3. Results and Discussion

Fig. 2 shows the Ig–t characteristics of $Al_{0.8}Sc_{0.2}N$ under positive and negative stress voltages applied to the top electrodes, and the time-to-breakdown (t_{BD}) can be determined by observing a rapid increase in gate current. Figs. 3(a) shows the Weibull distributions for $Al_{0.7}Sc_{0.3}N$ MFM devices. Note that the Weibull distribution depends on the stress polarity, and the Weibull slope (β) under positive bias is smaller compared to that under negative bias. Similar tendency can be seen in and $Al_{0.8}Sc_{0.2}N$ MFM devices, as shown in Fig. 3(b). It is inferred that the polarity dependence of the Weibull distribution is attributable to the asymmetry of AlScN films. In fact, a natively oxidized interfacial layer (IL) is formed near AlScN/top electrode interface. Fig. 4 shows the HAXPES analysis results confirming the natively oxidized IL at the AlScN top surface. It has been reported that oxygen from the oxidized top surface migrates along grain boundaries and extended defects in the AlScN layer, occupying nitrogen vacancies [4]. Furthermore, it is inferred that the quantity of nitrogen vacancies is associated with t_{BD} and the Weibull distribution. Based on these insights, the physical mechanism for the polarity dependence of the Weibull distribution may be attributed as follows. As shown in Fig. 5(a), oxygen ions or negatively charged oxygen within the native oxide IL infiltrate into AlScN film and fill nitrogen vacancies (V_N) under negative bias. Consequently, the apparent size of generated defects becomes smaller. On the contrary, as shown in Fig. 5(b), when the positive bias is applied to the top electrode, the oxygen infiltration is suppressed and the apparent size of generated defects becomes larger.

To verify this hypothesis, the plasma oxidation is performed on AlScN surfaces. Previous studies have reported that plasma oxidation preferentially oxidizes the Sc element, and the released nitrogen is pushed into and incorporated within the AlScN film [5,6]. Therefore, nitrogen vacancies may decrease, as shown in Figure 6. Actually, both the Al-O/Al-N and Sc-O/ScN intensity ratios increase following the plasma oxidation as shown in Fig. 4. Consequently, it has been demonstrated that the Weibull slope (β) under positive voltage is improved as shown in Fig. 7. It is conceivable that this fact may lend support to our expectation.

4. Conclusions

The TDDB characteristics in AlScN MFM devices are investigated from the statistical point of view. As results, the polarity dependence in the Weibull slope (β) is observed, and the plasma oxidation has a significant effect on this. Based on the experimental results, it can be concluded that there is a correlation between the amount of V_N and the redistribution of oxygeaaaan in AlScN films, as well as the TDDB statistics.

Acknowledgements

We would like to thank Mr. Arimitsu Kato (Tokyo Institute of Technology) for his great help in carrying out this research.

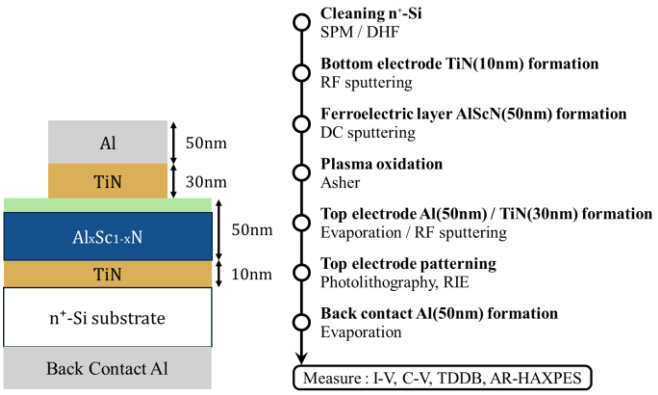

Fig.1 AlScN MFM structure used in this work.

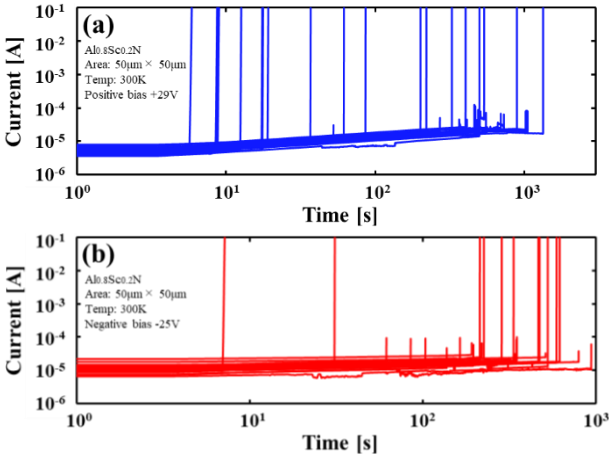

Fig2. Time-dependent dielectric breakdown (TDDB) characteristics for $Al_{0.8}Sc_{0.2}N$ under (a) positive bias +29V and (b) negative bias −25V on the top electrode.

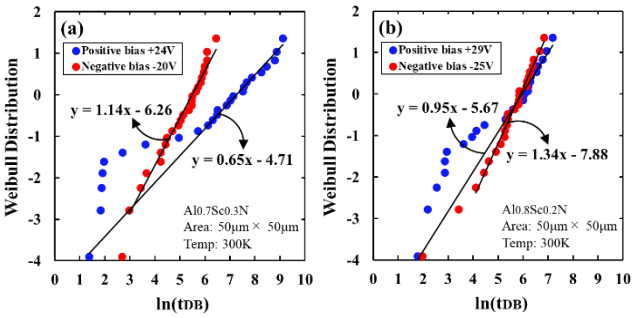

Fig3. Weibull distributions of (a) $Al_{0.7}Sc_{0.3}N$, (b) $Al_{0.8}Sc_{0.2}N$.

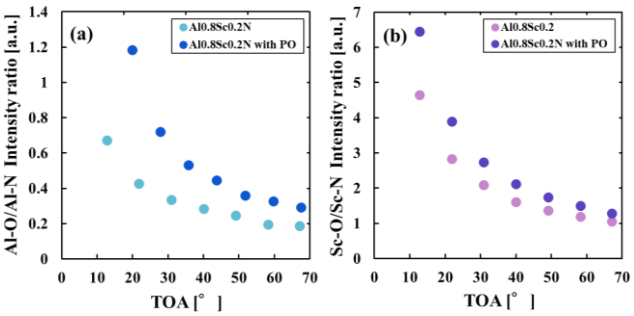

Fig4. AR-HAXPES results of (a) Sc–O/Sc–N and (b) Al–O/Al–N in $Al_{0.8}Sc_{0.2}N$ with and without plasma oxidation.

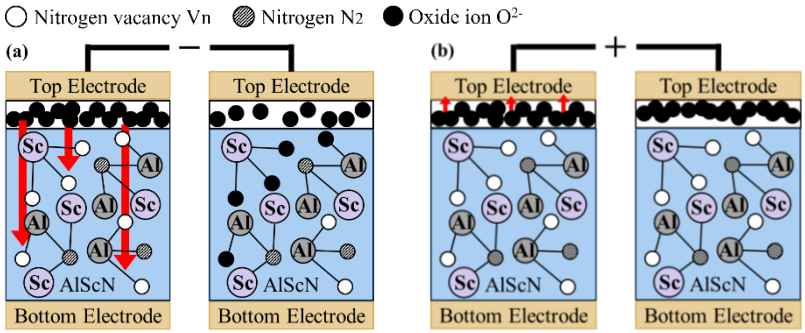

Fig5. Illustration of the mechanism by oxygen ion migration affecting TDDB variability under (a) negative and (b) positive top electrode voltage.

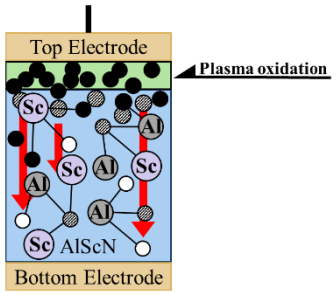

Fig6. Illustration of the mechanism suppressing variability in $Al_{0.8}Sc_{0.2}N$ with plasma oxidation.

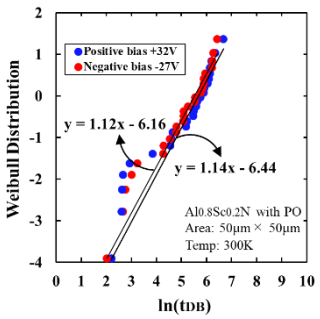

Fig7. Weibull distributions $Al_{0.8}Sc_{0.2}N$ with plasma oxidation.

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Estimation of Charge Trap Positions in Silicon Nitride Films Using Voltage-applied Hard X-ray Photoelectron Spectroscopy

Yoshiharu Kirihara[1], Hideyuki Yato[1], Yuichiro Mitani[1] and Hiroshi Nohira[1]
[1]Tokyo City University,
1-28-1 Tamazutsumi, Setagaya-ku, Tokyo 158-8557, Japan
Email: g2391202@tcu.ac.jp / Phone: +81-3-5707-0104

1. Introduction

Silicon nitride (Si_3N_4, hereafter referred to as SiN) films are used as charge trapped layers in three-dimentional NAND flash memory [1]. Previous studies have used electrical measurements to estimate the charge centroid and trap level of charges [2,3], but there are no studies that provide a physical evaluation of the distribution of charges trapped in SiN. In this study, in-situ voltage-applied angle-resolved hard X-ray photoelectron spectroscopy (AR-HAXPES) measurements were performed on devices with a metal-nitride-oxide-semiconductor (MNOS) structure, and the positions of charge traps were estimated by determining the potential distribution from the photoelectron spectrum shape.

2. Experimental Procedure

The experiment was performed on a SiN film of approximatly 5 nm deposited by chemical vaper deposition on a 5 nm-SiO_2/p-Si substrate. The raw materials are Dichlorosilane (DCS) or Hexachlorodisilane (HCDS). The sample preparation conditions are shown in Table 1. Different top electrodes were then deposited for C–V and HAXPES measurements. Electrical measurements were performed in a MNOS capacitor structure with Al electrodes deposited on both sides of the sample using a resistance heating evaporation method. The top electrodes for the HAXPES measurement samples were approximatly 10 nm Ni films deposited by resistance heating evaporation method. Voltage-applied AR-HAXPES measurements were performed at BL09XU of SPring-8 [4]. The Ni electrode was grounded, and a voltage was applied to the back contact of the p-Si(100) substrate. In the figure and text, the polarity of the applied voltage is indicated by the potential of the Ni electrode relative to p-Si(100) substrate. The N 1*s*, O 1*s*, Ni 2*p* and Si 1*s* photoelectron spectra were measured at a photoelectron take-off angle (TOA) range from 10° to 70°. The excitation X-ray energy of 7935 eV.

3. Results and Discussion

The C–V measurement results shown in Fig. 1 are for SiN samples produced from HCDS as the raw material. The flat-band voltage (V_{FB}) has shifted in the positive direction, indicating that electron trapping has occurred throughout the sample. The initial V_{FB} value is shifted more negatively than the value estimated from the work function difference between Al and p-Si(100), suggesting that hole may be present within the film as an initial charge. The HAXPES measurement results in Fig. 2 show that the Si 1*s* photoelectron spectra from SiN and SiO_2 shift before and after -7 V application. Figure 3 shows the V_{FB} calculated from the full width at half maximum (FWHM) of the SiO_2 peak. HAXPES measurements were performed while applying voltage, and the FWHM was determined using linear extrapolation. The result of determining the V_{FB} based on the intersection point was approximately -0.5 V. When comparing the V_{FB} obtained from C–V measurements with that obtained from HAXPES measurements, this V_{FB} is a reasonable value when considering the work function difference between Al and Ni. Figure 4 shows the chemical shift between p-Si(100) and SiN. Before voltage application, TOA dependence suggests that the surface region of the sample exhibits smaller chemical shifts compared to the interior, indicating that electrons may be confined within the SiN layer. Figure 5 shows the change in the binding energy of Si 1*s* photoelectrons from SiO_2 and SiN before and after voltage application. The shift of the SiN peak towards the high binding-energy side suggested either hole trapping or electron release. Considering the TOA dependence of the shift, it can be assumed that the charge is uniformly distributed within the SiN film. On the other hand, the SiO_2 peak is shifted in the opposite direction to the SiN peak, suggesting the possibility of counter charges occurring at the SiN/SiO_2 interface. From the perspective of charge centroid, electrical characteristics are greatly affected by charges existing at the SiN/SiO_2 interface rather than charges in the SiN film near the top electrode. Therefore, assuming that hole traps are uniformly distributed in the SiN film, the charge centroid becomes closer to the electrode, and the effect on the electrical characteristics becomes relatively small. This does not contradict the fact that electron traps are observed in the C–V measurement results.

4. Conclusions

In the C–V measurement, a positive V_{FB} shift was observed, confirming the presence of electron traps within the insulating film. HAXPES results indicate that holes are uniformly trapped in SiN films and that electron traps exist at the SiN/SiO_2 interface. Considering the charge centroid, this is consistent with the C–V measurement results.

Acknowledgements

The synchrotron radiation experiment was performed using the large synchrotron radiation facility BL09XU at SPring-8 with the approval of the Japan Synchrotron Radiation Research Institute (JASRI, Proposal Nos. 2023B1910, 2024A1595, 2024B2106, 2025A1803, 2025A1824 and 2025A2003).

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Table I The sample preparation conditions.

Materials	Temp. (°C)	Thickness (nm)
Dichlorosilane (DCS)	640	5
Hexachlorodisilane (HCDS)	700	5

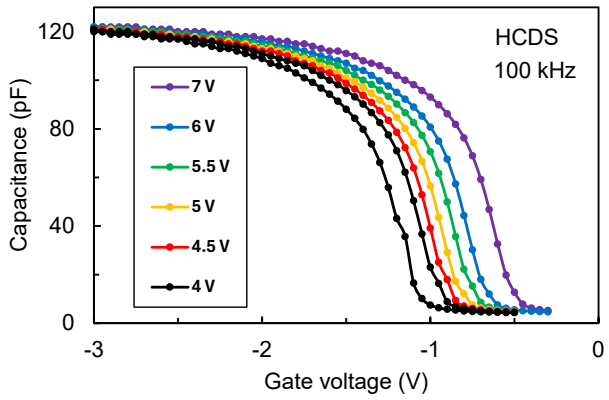

Fig. 1 The C–V measurement results of samples using HCDS.

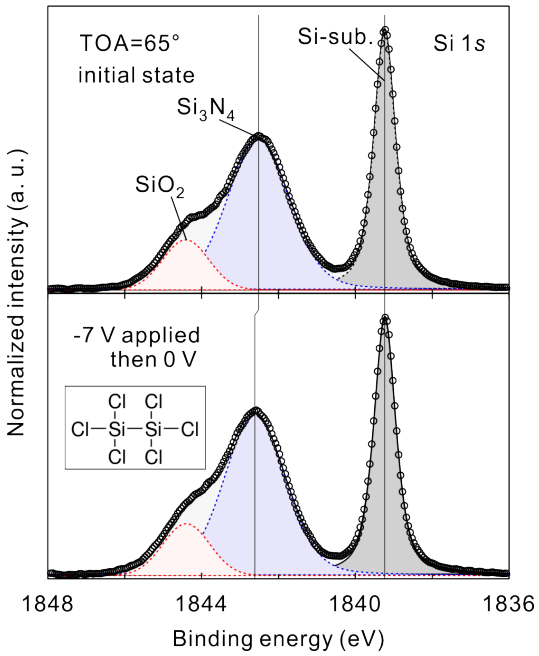

Fig. 2 Measurement results of Si 1*s* photoelectron spectroscopy spectra of samples using HCDS materials.

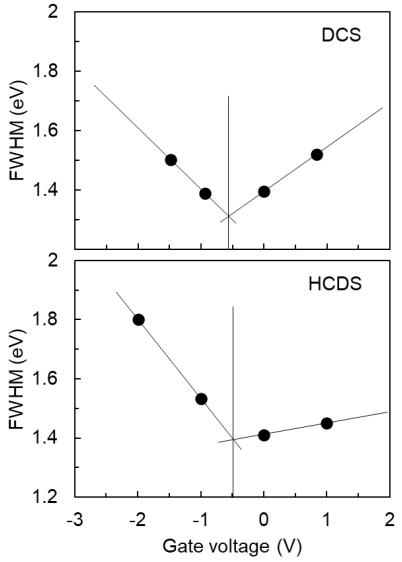

Fig. 3 Estimation of the flat band voltage from the voltage dependence of the FWHM of the SiO_2 peak.

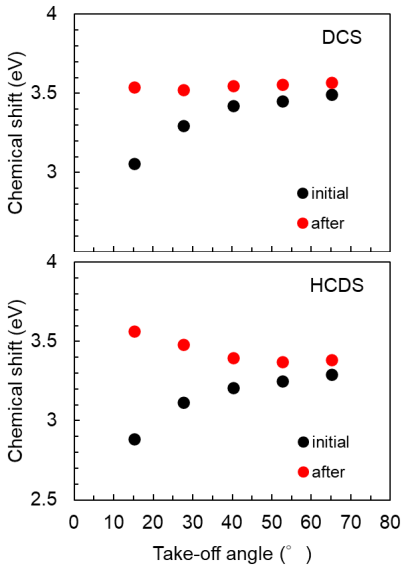

Fig. 4 Chemical shift between SiN peak and p-Si(100) substrate peak before and after voltage application.

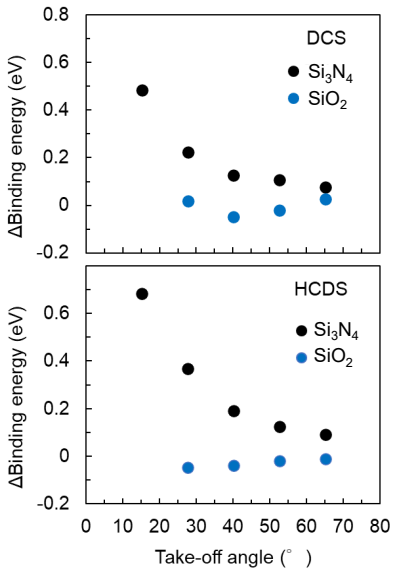

Fig. 5 Changes in the binding energy of SiN peaks and SiO_2 peaks before and after voltage application.

Fabrication of non-volatile memory using Al_2O_3/spin-coated CeO_x/SiO_2/Si stack

Hiroaki Tanaka[1], Yoshiharu Kirihara[1], Sorato Mikawa[1], Tomoki Yoshida[1],
Ryousuke Ishikawa[1] and Hiroshi Nohira[1]
[1]Tokyo City University, 1-28-1 Tamazutsumi, Setagaya-ku, Tokyo 158-8557, Japan
Email: g2581261@tcu.ac.jp / Phone: +81-3-5707-0104

1. Introduction

Non-volatile memory devices utilizing oxide materials have attracted significant attention. Recently, interface dipole modulation (IDM) has been observed in amorphous HfO_2/atomic layer deposited (ALD) TiO_x/SiO_2 stacked structures [1,2]. The IDM modulation layer has also been observed in SnO_x, and it is expected to occur in other multivalent oxides [3]. However, this stacked structure is similar to flash memory that uses a SiN film as a charge-trapping layer, suggesting the possibility that charges could be trapped in the modulation layer [4]. In this study, cerium oxide (CeO_2) was introduced as a novel modulation layer material, and unlike conventional ALD methods, CeO_2 films were fabricated using a cost-effective spin-coating process [5]. Specifically, CeO_2 film uniformity was evaluated by scanning electron microscopy (SEM), and the mechanism of the memory operation was examined through capacitance–voltage (C–V) measurements and hard X-ray photoelectron spectroscopy (HAXPES).

2. Experimental Procedure

Figures 2(a) and 3(a) show the structures of the measured samples. A 10 nm thick SiO_2 film was thermally grown on an n-Si(100) substrate, followed by spin coating of a 0.3 nm thick CeO_x film. The CeO_x layer was dried on a hot plate at 300 °C for 3 minutes. Subsequently, a 5.0 nm Al_2O_3 layer was deposited by atomic layer deposition (ALD), followed by a post-annealing process at 450 °C for 30 minutes under a nitrogen atmosphere. Different top electrodes were then deposited for C–V and HAXPES measurements. The top electrodes for the HAXPES measurement samples were 4 nm Ni films deposited by vacuum evaporation. Voltage-applied HAXPES measurements were performed at BL09XU of SPring-8. The gate electrode was grounded, and a voltage was applied to the back contact of the n-Si(100) substrate. The Ni 2*p*, Ce 3*d*, Al 1*s*, and Si 1*s* photoelectron spectra were measured at a photoelectron take-off angle (TOA) of 85° relative to the sample surface with an incident X-ray energy of 7935 eV. For C–V measurements, Al top electrodes were deposited by vacuum evaporation, and a sweeping voltage up to 10 V at a frequency of 1 MHz was applied.

3. Results and Discussion

SEM observation shown in Fig. 1(a) revealed that the CeO_x film deposited by spin coating existed in an island-like form. Figure 1(b) shows the relationship between solution concentration and average CeO_x film thickness. This film thickness calculation was performed using X-ray photoelectron spectroscopy (XPS) and shows the results calculated from the intensity ratio of Ce 3*d* photoelectrons from CeO_x and Si 2*p* photoelectrons from the Si substrate. Figure 1(c) shows that the proportion of Ce^{3+} increases as Al_2O_3 is deposited. The results of the C–V measurement shown in Fig. 2(a) indicate counterclockwise hysteresis. The hysteresis width increased with voltage, as shown in Fig. 2(b), reaching a maximum of approximately 0.77 V. These results suggest that the trapped charge is likely a hole, as indicated by the band alignment shown in Fig. 2(c). Furthermore, the trapping site is considered to be the island-like CeO_x. Figure 3(a) shows the results of HAXPES. The application of voltage shifted the photoelectron peaks of Si 1*s* and Al 1*s* in the same direction. This phenomenon is consistent with the trapping of holes in the CeO_x layer. Furthermore, the TOA dependence of the intensity ratio of the photoelectron spectra from Ce 3*d* and Al 1*s* shown in Fig. 3(b) indicates that CeO_2 does not diffuse into the upper Al_2O_3 layer and maintains a bilayer structure.

4. Conclusions

C–V and HAXPES measurements were performed on the metal/$Al_2O_3/CeO_x/SiO_2$/Si structure. The results indicate that the spin-coated CeO_2 layer forms island-like structures, which act as charge-trap sites for memory operation.

Acknowledgments

This work was partly supported by TOKYO CITY UNIVERSITY Interdisciplinary Research Center for Nano Science and Technology for instrumental analysis. The synchrotron radiation experiment was performed using the

large synchrotron radiation facility BL09XU at SPring-8 with the approval of the Japan Synchrotron Radiation Research Institute (JASRI, Proposal Nos. 2025A1803 and 2025A1824).

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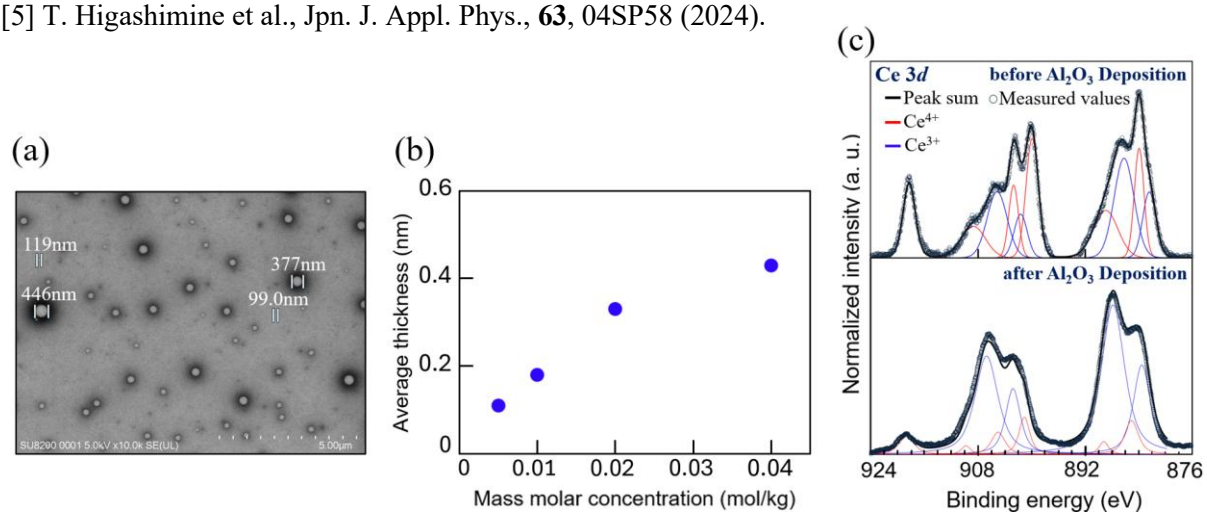

Fig. 1. (a) SEM image. (b) Film thickness dependence on solution concentration. (c) Changes in CeO_x bonding state after Al_2O_3 deposition.

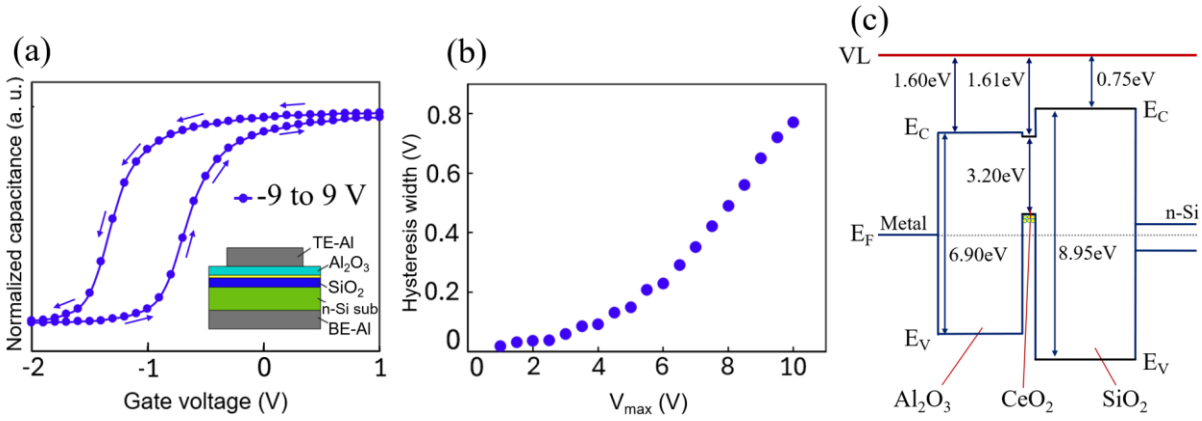

Fig. 2. (a) C–V measurement. (b) Voltage dependence of hysteresis width. (c) Band alignment of stacked structure.

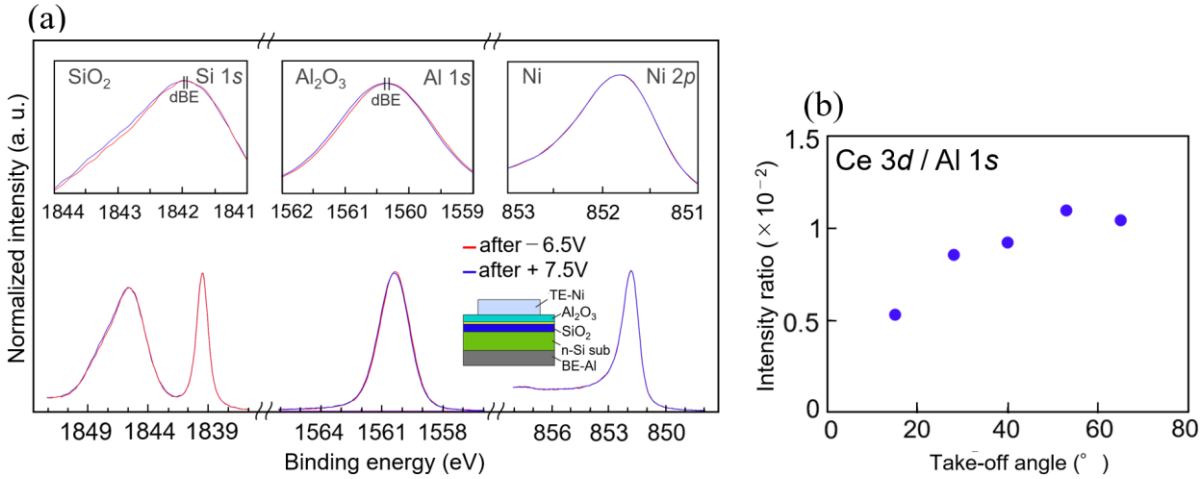

Fig. 3. (a) Changes in binding energy of Si 1*s*, Al 1*s*, and Ni 2*p* photoelectrons before and after voltage application. (b) Take-off angle (TOA) dependence of the photoelectron intensity ratio (Ce 3*d*/Al 1*s*).

New SOD for Crack-Free Thick Film

Ikuya Ichie[1], Kensuke Aida[1], Kousuke Kabasawa[1], Ryo Sasaki[1], and Naoko Nakamoto[1]

[1]Merck Electronics Ltd.

[1]3330 Chihama, Kakegawa-shi, Shizuoka-Pref. 437-1412, Japan

Email: naoko.nakamoto@merckgroup.jp / Phone: +81-537-77-2219

1. Introduction

Spin on dielectrics (SOD) allows for film formation through a simpler process compared to CVD and ALD, since the films can be deposited using a coating track instead of using vacuum deposition tools. Among these, perhydropolysilazane (PHPS) is widely used in applications such as NAND and DRAM [1]. In modern devices, as three-dimensional structures become more prevalent, there is an increasing demand for film formation on deeper patterns [2]. However, with conventional PHPS cracks tend to occur when embedding films thicker than approximately 1 µm or in trenches with a high aspect ratio [3]. The purpose of this study is to develop a novel SOD polymer for SiO_2 and its process to form significantly thicker films in deeper structures.

2. Experimental Procedure

Sample A is a novel SOD functional material synthesized based on conventional PHPS polymer. Conventional PHPS and Sample A were spin-coated onto a 4 inch bare Si wafer to form a film thickness of 2.5 µm. SiO_2 film was formed by post-coat baking at a low temperture, curing in a steam atmosphere a medium temperatiure to convert the PHPS to SiO_2 and in an N_2 atmosphere at a high temperature to complete the SiO_2 conversion and densify the film. Sample A was spin-coated onto a patterned substrates with 16 µm depth and subjected to 3 different processes to form an SiO_2 film- (a) the conventional process mentioned above, (b) baking at a lower temperature compared to conventional process, followed by catalyst gas and steam atmosphere pre-treatment (X), steam cure at a medium temperature range and ending with a final anneal in N_2 atmosphere at high temperature and (c) baking at a lower temperature compared to conventional process, followed by evaporation suppression pre-treatment (Y), a steam cure at medium temperature and ending with a final anneal in N_2 atmosphere high temperature. The samples for the measurement of basic film properties were prepared under the conditions specified in Table I. The density within the pattern was evaluated by etching the cross-section with dilute HF and observing the etching behavior using SEM.

3. Results and Discussion

Fig.1 shows the images of films formed from PHPS and Sample A. PHPS exhibited massive cracking across the entire surface, while Sample A was coated without any cracks. Sample A exhibited reduced cracking by incorporating a cross-linked structure with additives. Table I shows, Sample A exhibited lower shrinkage and stress compared to conventional PHPS. It is seen that the lower baking temperature and the pre-treatment using catalyst gas treatment process resulted in reduced shrinkage and stress compared to the conventional process. The pre-treatment in the evaporation suppression treatment process further reduced shrinkage and stress. Fig. 2 shows optical micrographs and cross-sectional SEM images of the trenches after coating Sample A and curing using the conventional process, after catalyst gas treatment, and after evaporation suppression treatment. These results indicate that the SiO_2 films subjected to pre-treatment exhibit improved crack resistance during trench filling and enhanced film density within the trench.

4. Conclusions

By applying Sample A to the interlayer dielectric film and performing catalyst gas treatment or evaporation suppression treatment, it was demonstrated that it can also be adapted to larger structures.

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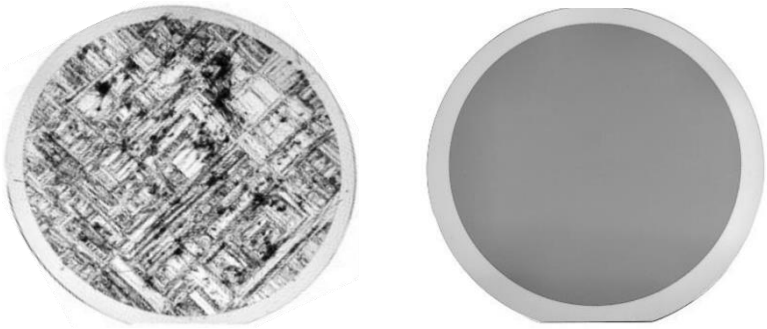

Fig.1 Film thickness:2.5 um,
After high temp in N_2 curing, left : conventional PHPS, right : Sample A

Table I Film properties

Sample	Process			Shrinkage (Bake to cure)	Stress (MPa) after cure
	Dry bake	Pre-treatment	Curing		
PHPS	Low temp in Air		Medium temp in H_2O High temp in N_2	23.6%	6.2
Sample A	Low temp in Air		Medium temp in H_2O High temp in N_2	22.5%	-44.4
Sample A	Low temp in Air	Catalyst gas (X) + H_2O	Medium temp in H_2O High temp in N_2	20.0%	-74.2
Sample A	Low temp in Air	Evaporation suppression (Y)	Medium temp in H_2O High temp in N_2	10.5%	-97.4

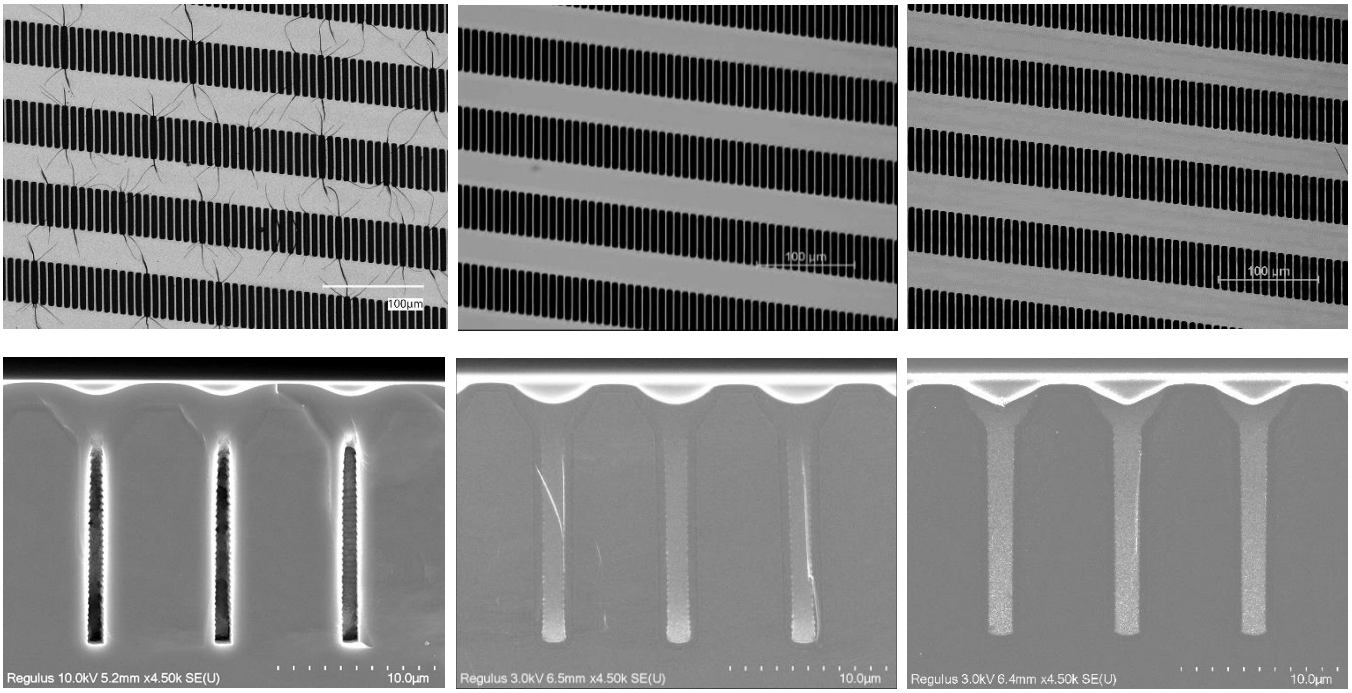

Fig. 2 Left : Conventional process, Center : Catalyst gas process (X), Right : Evaporation suppression process (Y)

Profile-Based Modeling of AC Stress-Induced Degradation in SiON pMOSFETs

Kyungmin Yoon[1], Donghee Son[2], and Yeohyeok Yun[1*]
[1]KOREATECH, [2]Samsung Electronics,
[1]1600 Chungjeol-ro, Byeongcheon-myeon, Dongnam-gu, Cheonan-si, Chungcheongnam-do, 31253, Republic of Korea
Email: yhyun@koreatech.ac.kr / Phone: +82-41-560-1175

1. Introduction

SiON MOSFETs are still widely used in modern circuits such as CMOS inverters. Nevertheless, reliability issues such as AC stress-induced degradation remain critical, especially due to the interaction between ON-state (NBTI) and OFF-state stress [1]. This paper investigates how degradation in the preceding stress phase affects subsequent phases and proposes an improved model incorporating post-ON/OFF degradation. The model accurately predicts ΔV_{th} by combining degradation profiles across channel regions under different duty ratios.

2. Experimental Procedure

The device under test was a planar p^+ poly-Si gate pMOSFET with channel width $W = 0.47$ μm, channel length $L = 47$ nm and a SiON gate dielectric with an EOT of 2.2 nm.- The AC stress was applied with $V_{dd} = -2.5$ V, duty cycles ranging from 10% to 75%, $f = 100$ kHz, and $T = 398$ K. ON-state stress was applied using $V_g = -2.5$ V, and OFF-state stress was applied using $V_d = -2.5$ V, with all other terminals grounded. The V_{th} was extracted using the constant current method ($J_d = 1$ μA/μm) [2]. All electrical measurements were performed using an Agilent B1500A semiconductor device analyzer with a B1530A waveform generator.

3. Results and Discussion

The measured ΔV_{th} under AC stress strongly depended on the duty ratio. As shown in Fig. 1, ΔV_{th} remained positive at duty ratios below 50% because OFF-state degradation dominated through negative charge trapping near the drain edge [3]. With increasing duty ratio, the influence of ON-state stress became more evident, as positive charges generated across the channel reduced ΔV_{th} degradation [3]. This behavior is summarized in Fig. 2, where the data at t_s = 2,000 s followed an exponential dependence on duty ratio, indicating that AC degradation can be approximated by combining the effective durations of ON- and OFF-state stresses.

The summation of ΔV_{th} contributions from ON- and OFF-state stresses at their effective durations was compared with the measured ΔV_{th} under AC stress, as shown in Fig. 3. The discrepancy between the two indicates that the location of defects generated by ON- and OFF-state stresses governs the degradation behavior. Therefore, the spatial degradation profiles of these stresses must be taken into account when analyzing the AC degradation mechanism.

Fig. 4 and Fig. 5 indicate that ON-state stress generated positive charges along the entire channel, particularly near the source/drain edges, while OFF-state stress induced localized negative charges at the drain edge [4]. These differences demonstrate that degradation profiles must be considered rather than simply adding the two stress components. The influence of pre-stress on subsequent degradation was also evident. As illustrated in Fig. 4, post-ON degradation became more severe after a pre-OFF cycle because the prior traps increased the oxide electric field (E_{ox}). Likewise, Fig. 5 shows that post-OFF degradation was enhanced after a pre-ON cycle due to a higher gate–drain field at the drain edge (E_{gd}). These effects were modeled as $\Delta V_{th} = A_0 \exp(\beta E_{ox}) t^n$ and $\Delta V_{th} = A_0 \exp(\gamma E_{gd}) t^n$ for each region and each stress phase.

Finally, the validity of the proposed model is demonstrated in Fig. 6, where the calculated ΔV_{th}, obtained by combining post-ON and post-OFF contributions over their effective stress durations, agreed well with experimental results across all duty ratios. These results show that AC degradation in SiON pMOSFETs can be reliably predicted from DC stress data by incorporating degradation profiles and stress interactions that can be extracted from *I–V* measurements.

4. Conclusions

An advanced AC degradation model for SiON *p*MOSFETs was proposed by explicitly considering the spatial degradation profiles of ON- and OFF-state stresses. The proposed method considers the mutual interaction between pre- and post-stress mechanisms, resulting in accurate ΔV_{th} predictions under varying duty ratios. This modeling approach enhances the reliability of lifetime predictions for SiON devices and provides insights that may be applicable to other gate dielectric technologies.

Acknowledgements

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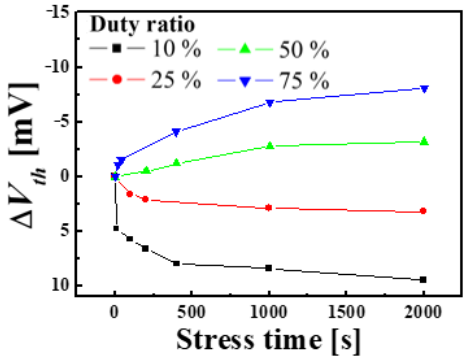

Fig. 1. ΔV_{th} vs. t_s of *p*MOSFET during AC stress at d_t = 10, 25, 50, 75 %.

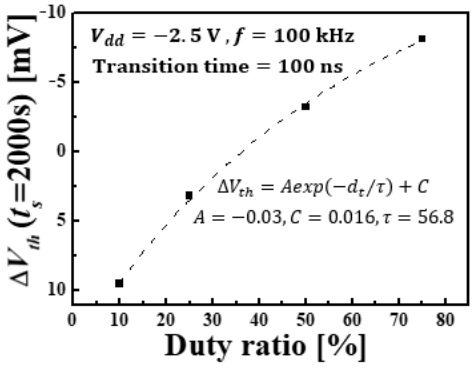

Fig. 2. ΔV_{th}(t_s = 2,000 s) vs. d_t of *p*MOSFET due to AC stress.

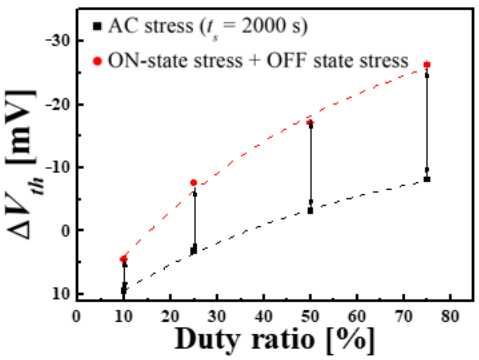

Fig. 3. Comparison of ΔV_{th}s due to AC modeling and measurement

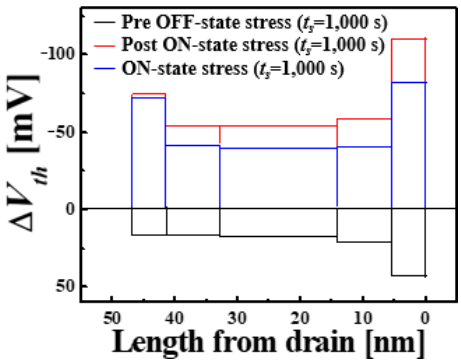

Fig. 4. The degradation profile of OFF-state stress, ON-state stress and post-ON-state stress after OFF-state stress (Each t_s = 1,000 s).

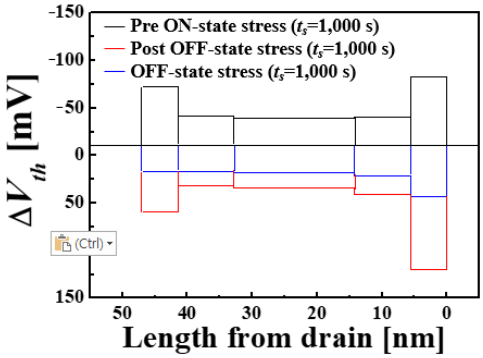

Fig. 5. The degradation profile of ON-state stress, OFF-state and post OFF-state stress after ON-state stress (Each t_s = 1,000 s).

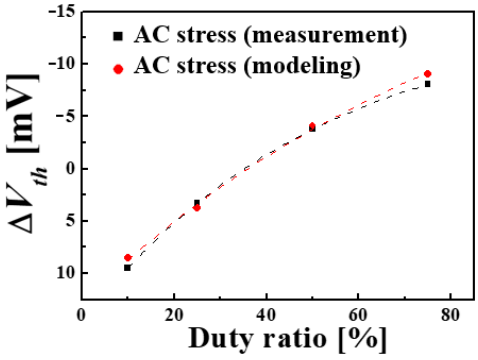

Fig. 6. The measured and modelled total $\Delta|V_{th}|$s due to AC stress at different duty ratio.

New Insights into MOS Interface Degradation of pMOSFETs and nMOSFETs at Cryogenic Temperature

Yuta Horiko, Yutaro Masukawa, and Yuichiro Mitani
Tokyo City University
1-28-1 Tamazutsumi, Setagaya-ku, Tokyo 158-8557, Japan
Email: g2481275@tcu.ac.jp / Phone: +81-3-5707-0104

1. Introduction

In recent years, the importance of CMOS technology capable of operating under cryogenic environments has been increasing in fields such as quantum computing and space development. While CMOS operation at cryogenic temperatures opens up new possibilities for applications, many aspects of MOSFET interface properties and device reliability remain unclear. In particular, the degradation mechanisms of the MOS interface under cryogenic conditions have not yet been fully elucidated [1]. Concurrently, it is imperative to ensure the reliability of both pMOSFETs and nMOSFETs, which constitute CMOS circuits. In this study, we investigate and compare the characteristics of interface degradation in pMOSFETs and nMOSFETs under cryogenic temperature, and discuss their respective degradation mechanisms.

2. Experimental Procedure

Fig. 1 shows the measurement sequence and the device structure. The device in this work were pMOSFETs and nMOSFETs with 6nm of gate oxides thickness, the gate width and length are 100μm and 2μm, respectively. As shown in Fig. 1(a), the interface state densities of pMOSFETs and nMOSFETs were evaluated using the charge pumping method [2]. Here, the temperature dependences of the respective parameters (*i.e.* intrinsic carrier density, thermal velocity, and capture cross sections) are considered [3, 4]. The electrical stress was applied under the conditions of Fowler–Nordheim (FN) tunnelling at V_G = –8.8 V for pMOSFETs and V_G = 7.0 V for nMOSFETs. These voltages correspond to J_G = 0.01 A/cm², and were chosen to equalize the amount of charge flowing during stress between pMOSFETs and nMOSFETs.

3. Results and Discussion

Fig. 2 shows the stress time evolutions of the I_D–V_G characteristics for pMOSFETs and nMOSFETs at 300 K and 77 K. The shift in the I_D–V_G characteristics induced by FN stress is suppressed at low temperatures in both pMOSFETs and nMOSFETs. Furthermore, the degradation in nMOSFETs is found to be more suppressed at lower temperature in comparison to that of nMOSFETs. Fig. 3 shows the stress time evolutions of ΔIon (at Vth±1V). ΔIon degrades more seriously with increasing temperatures. And the Ion degradation in pMOSFETs is significantly more pronounced than that observed in nMOSFETs at lower temperatures. Fig. 4 shows the temporal progression of stress over the generated interface (ΔDit) at varying temperature. Interface-state generation in nMOSFETs shows a considerable degree of temperature dependence with ΔDit being suppressed at lower temperature compared to that observed in pMOSFETs. In our previous reports, the correlation between ΔIon and ΔDit has been observed, even at lower temperature. In a similar manner, the correlations between ΔIon and ΔDit for pMOSFETs and nMOSFETs within the temperature range from 60 K to 300 K are shown in Fig. 5, It is observed that the slopes of nMOSFETs become steeper below approximately 150 K. This result may imply that the predominant degradation mechanism changes at approximately this temperature. The temperature dependences of ΔDit following 32-sec FN stress in both nMOSFETs and pMOSFETs are plotted in Fig. 6. From Fig. 6, the activation energies both MOSFETs exhibit a change at temperatures ranging from approximately 100 ~ 125 K. According to the previous literature [5], NBTI effects have been documented as being reduced below 150 K. Although Further investigations are required to understand the underlying physics behind this result, the temperature dependences of hydrogen bond dissociation and/or these diffusion may be associated with interface-state generation.

4. Conclusions

The interface-state generation in MOSFETs under FN stress depends on the temperature. And the dominant degradation mechanism at the cryogenic temperature exhibit a change. Furthermore, these degradation mechanisms these degradation mechanisms may differ between nMOSFETs and pMOSFETs.

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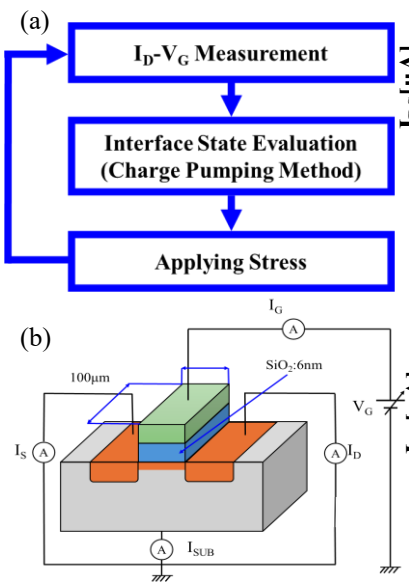

Fig. 1 (a)Measurement sequence for I_D-V_G characteristics and interface states, (b) device structure and measurement configuration used in this work.

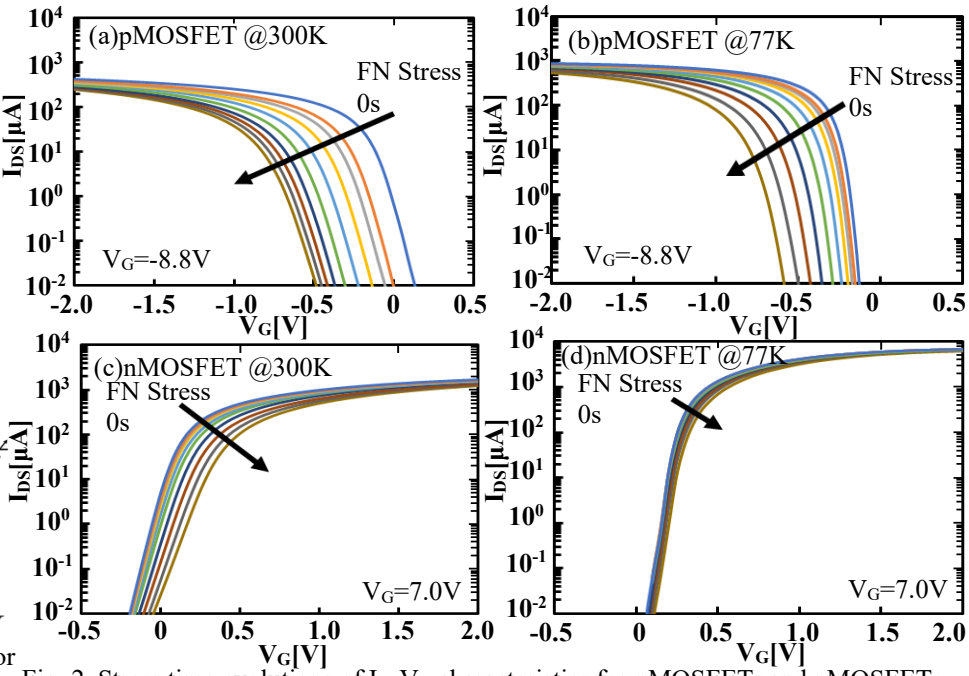

Fig. 2 Stress time evolutions of I_D-V_G characteristics for pMOSFETs and nMOSFETs (a)pMOS 300K, (b)pMOS 77K, (c)nMOS 300K, (d)nMOS 77K. The device size was W/L=100/2μm, and the stress were applied at V_G = -8.8 V for pMOS and V_G = 7.0 V for nMOS.

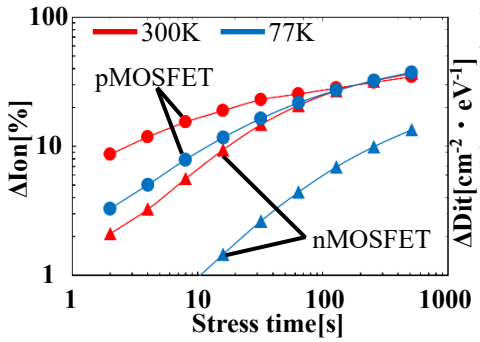

Fig. 3 Ion degradation (ΔIon) versus stress time at different devices and temperatures.

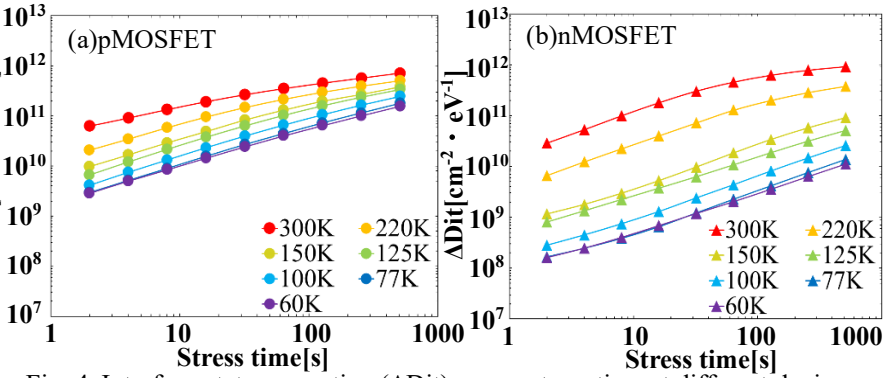

Fig. 4 Interface-state generation (ΔDit) versus stress time at different devices and temperatures.(a)pMOSFET, (b)nMOSFET.

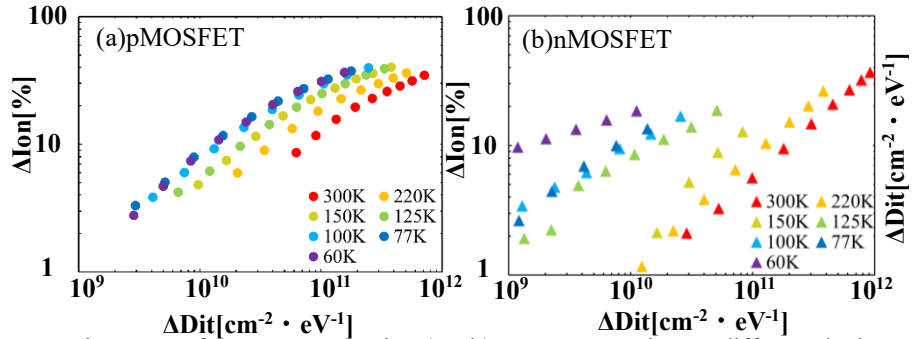

Fig. 5 Interface-state generation (ΔDit) versus stress time at different devices and temperatures. (a)pMOSFET, (b)nMOSFET.

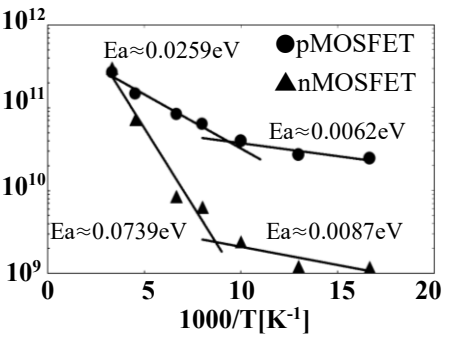

Fig. 6 Arrhenius Plot of interface-state generation (ΔDit) for nMOSFET and pMOSFET after 32s Stress.

Nondestructive inspection of SiO2/Si interface defect density by nonlinear optics

Kuang-Yao Lo[1,*], Hua-Hsing Liu[1], Ting-Yu Yen[1], Chiu-Hsien Wu[2], and Kung-Ming Hung[3]
[1] Dep. of Physics, National Cheng Kung Univ., 701 Tainan, Taiwan
[2] Dep. of Physics, National Chung Hsing Univ., 402 Taichung, Taiwan
[2]Dep. of Electronic Engineering, National Kaohsiung Univ. of Science and Technology, 807 Kaohsiung, Taiwan
*E-mail: kuanglo@mail.ncku.edu.tw / Phone : +886-6-2757575-65261

1. Introduction

The growing demand for advanced field-effect transistors (FETs) in contemporary technology necessitates ongoing efforts to reduce device dimensions and streamline fabrication procedures.[1] Key developments, such as FinFETs and gate-all-around (GAA) FETs, have been driven by requirements for enhanced portability and improved energy efficiency.[2] As FETs continue to shrink to the nanoscale, surface and interface effects become increasingly significant. The defects arise from broken or imperfect bonds, dangling bonds, or impurities, and they play a critical role in semiconductor device performance. These defects act as centers for charge trapping and scattering, significantly degrading the device's electrical performance by affecting its speed, efficiency, and stability[3]. The interface defect density (Dit) is a crucial parameter for characterizing the quality of semiconductor-dielectric interfaces, and reducing Dit is a key goal in device fabrication processes. While accurately determining Dit are essential for predicting manufacturing yields, traditional electrical measurement methods used in current semiconductor fabrication processes can be destructive and excessively time-consuming, sometimes extending over several months. This significantly delays the optimization of manufacturing parameters. Consequently, there is an urgent need for the development of innovative, real-time methods to ensure precise doping control and accurately measure Dit, thereby facilitating improved transistor fabrication and device performance. This bottleneck underscores the need for a fast, non-destructive alternative for real-time Dit characterization.

In this study, we propose a nonlinear optical technology, second harmonic generation (SHG) as an optical approach for efficient Dit detection. SHG method is a non-destructive optical technique, is highly sensitive to the symmetric structure of surfaces and interfaces, as well as the location of defects therein, making it a useful tool for characterizing doping profiles in semiconductor materials.[4]. Based on analysing time dependent SHG (TD-SHG) signals, we develop a comprehensive model that accounts for the evolution of charge density and corresponding quantum tunnelling effects. Through this framework, we built a simplified equation that accurately fits experimental data. This advancement not only enhances fabrication efficiency but also paves the way for real-time monitoring and optimization of semiconductor devices, facilitating the development of next-generation electronic components.

2. Experimental Procedure

A TD-SHG system with a vacuum chamber is exhibited in Fig.1. This experiment has to perform in a controllable vacuum environment to tune the suitable oxygen pressure for surface charge traps on SiO_2 surface. The light source of this experiment is a femto second laser with the wavelength of 1044 nm and the duration of 100 fs. The detailed system setup and performance refers Ref.4. The sample conditions are listed in Tab.1

3. Results and Discussion

Due to performing in the high-vacuum environment and considering the thickness of the oxide layer, electron transmission and trapping at the SiO_2 surface are obviously hindered.[5] In the TD-SHG experiments, three-photon absorption excites bound electrons to a high-energy state via femto second laser pumping, which then tunnel into defect states in the SiO_2 layer, as the energy band-edge energies of Si/SiO_2, thereby forming a quasi-static DC electric field ($\overrightarrow{E_{DC}}$), as shon in Fig.2. Therefore, the third order susceptibility ($\chi^{(3)}$) dominantly changes the SHG intensity, which is defined as electric-field-induced second harmonic generation (EFISHG). For simplifying, TD-SHG signal can be expressed as Eq.(1)

$$I^{2\omega} = \left| X_2 e^{i(Im)*\frac{\pi}{180}} + E_0\left(1 - e^{-\frac{t}{t_0}}\right) + E_1\left(1 - e^{-\frac{t}{t_1}}\right)\right|^2 \quad (1)$$

Where, $X_2 e^{i(Im)*\frac{\pi}{180}}$ is the complex of $\chi^{(2)}$ and also contains the intrinsic defects in the SiO_2/Si. E_0 and E_1 contain the coefficient $\chi^{(3)}$. The time constant, t_0, is related to the interface traps and The time constant, t_1, is a function of peak power. The value of E_0 is directly related to Dit.

To obtain Dit, we measured the TD-SHG spectra of samples S1–S3 are shown in **Fig.3**. The solid lines in **Fig.3** are the curves simulated using the PINN method. According to **Eq. 1**, the parameter E_0 is expected to be proportional to the total trap density. To further validate this relationship, we performed conductance-voltage (G-V) analysis to extract Dit, with the results summarized in **Tab.1**. These findings support the feasibility of SHG-based techniques as a reliable and non-invasive alternative for interface trap characterization.

Herein, we introduce transfer learning in a physics informed neural network (PINN) to exploit the inherent similarities across datasets [6]. Fig. 4 shows the relationship between the averaged E_0 obtained by TD-SHG and Dit measured by G-V method, that is, $E_0 = \alpha \cdot \log(Dit)$. The increasing trend indicates that there is a correlation between E0 and the interface trap density Dit, suggesting that E_0 can be used as an optical indicator of Dit and is consistent with the results of electrical measurements. This approach improves computational efficiency while ensuring the physical consistency of the model, and is particularly suitable for real-time optical characterization and semiconductor component analysis.

4. Conclusions

This work demonstrates a fast, non-invasive method for Dit extraction, offering a promising alternative to conventional electrical measurements. The integration of SHG-based optical techniques with deep learning provides an efficient approach for real-time semiconductor interface characterization, paving the way for advanced non-destructive Dit measurements in semiconductor manufacturing.

Acknowledgements

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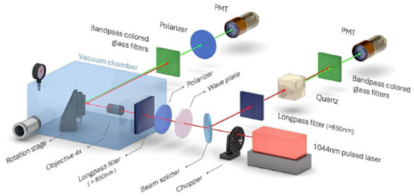

Fig. 1 TD-RSHG experiment system.

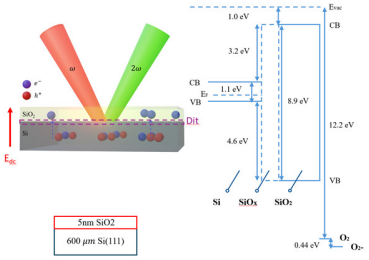

Fig. 2 TD-SHG and band diagram on SiO_2/Si.

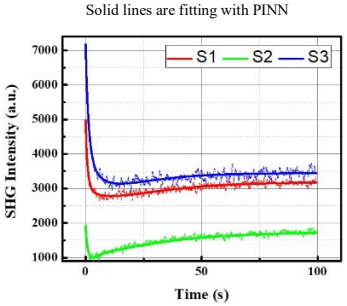

Fig.3 The TD-SHG spectra

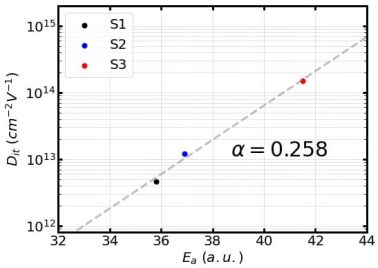

Fig. 4 The relationship between E_0 and Dit.

Sample	Treatment	Dit ($cm^{-2}V^{-1}$)	E_0(a.u.)
S1	As growth	$4.6x10^{12}$	35.8
S2	H_2O 0.5ml+200 atm CO_2, 1hr, 573K	$1.2x10^{13}$	36.9
S3	5 psi NF3+90 atm N_2, 1hr, 573K	$1.5x10^{14}$	41.5

Tab. 1 Sample treatment details, the corresponding Dit and E_0

High-Performance Ge FinFET CMOS Devices with Low-Temperature Supercritical Fluid Process after Post-Plasma Oxidation and Nitridation Treatments

Yu-Ren Lin[1], Kuei-Shu Chang-Liao[1,2*], Kai-Chun Yang[2]
[1]College of Semiconductor Research, [2]Department of Engineering and System Science,
National Tsing Hua University, Hsinchu 30013, Taiwan, R.O.C.
*E-mail: lkschang@ess.nthu.edu.tw

1. Introduction

Germanium (Ge) is a promising channel material due to its high carrier mobility [1], [2], but challenges remain, particularly the unstable oxidation states at the interfacial layer (IL) [3], [4]. A low-temperature supercritical fluid (SCF) treatment has recently been proposed to address these issues by passivating oxygen vacancies without increasing EOT or damaging the high-k layer [5]. SCF combines gas-like penetration and liquid-like solubility, enabling uniform and effective delivery of oxidants to the IL surface [6]. The impact of post-plasma treatments on the gate stacks is investigated to further enhance the effectiveness of SCF treatment.

2. Experimental Procedure

The Ge MOS capacitors were fabricated on p-type Ge (100) wafers with resistivity of 1-10 ohm-cm, while the Ge FinFET CMOS inverter was fabricated on 8-inch SOI wafer with 80 nm epitaxial Ge layer on the top. After the high-k gate stacks formation, post-plasma oxidation (PPO) and nitridation (PPNO) treatments were carried out. Afterwards, a low-temperature supercritical fluid (SCF) hydroxide oxidation treatment was applied, while the treated samples were named as control SCF, PPO+SCF, and PPNO+SCF. Then, the standard MOS capacitor and FinFET process flows were continued to complete the device fabrication.

3. Results and Discussion

In Fig. 1 of the cross-sectional TEM image and EDS mapping, the fin structure consists of single-crystal Ge with height of 50 nm, width of 30 nm and length of 80 nm. In Fig. 2 of the XPS of O1s spectra and deconvolution analysis, the oxygen-vacancy bonds are evidently reduced with post-plasma oxidation treatment. However, the post-plasma nitridation treatment increases the oxygen vacancy concentration. It is believed that some unstable oxidation states and traps are passivated by triple bonds from nitrogen atom, which can't be observed from O1s deconvolution analysis. In Fig. 3 of the comparison of J_G-EOT, all the samples follow the scaling trend, while the EOT values are around 0.6 nm and the J_G can be suppressed to 10^{-4} A/cm^2, simultaneously. In Fig. 4 of the frequency dispersion of C-V curves, both border and interface traps can be reduced with PPNO+SCF treatment. Results indicate that the triple bonds from nitrogen treatment have passivated most shallow traps located in gate stacks, or the interface between high-k and IL, which significantly enhances the effectiveness of a SCF treatment. In Fig. 5 of the I_D-V_G curves, the values of S.S. and I_{ON}/I_{OFF} in both n-type and p-type Ge FinFET are significantly improved by a PPNO+SCF treatment, which may be attributed to the simultaneous reduction of interface trap and gate leakage. In Fig. 6 of the I_D-V_D curves, the drive current for Ge pFinFET is three times higher than that of Ge nFinFET. For the V_{OUT}-V_{IN} curves of Ge FinFET CMOS inverter shown in Fig. 7, the symmetrical V_{IN}-V_{OUT} characteristics could be improved by balancing the influence from oxidation and nitridation.

4. Conclusions

In conclusion, to enhance the effectiveness of a SCF treatment, an additional post-plasma oxidation and nitridation treatments was applied on high-k gate stacks of Ge FinFET before standard SCF treatment. Due to the triple bonds from nitrogen treatment, most shallow traps located in gate stacks, or the interface between high-k and IL, have been passivated. As a result, both Ge nFinFET and pFinFET with PPNO+SCF treatment exhibit higher I_{ON}, lower I_{OFF}, larger I_{ON}/I_{OFF}, lower S.S. and D_{IT} value.

Acknowledgements

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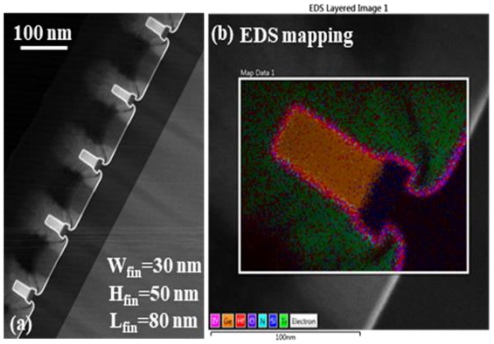

Fig. 1 (a) TEM image and (b) EDS mapping of Ge FinFET with post-plasma nitridation and supercritical fluid treatment.

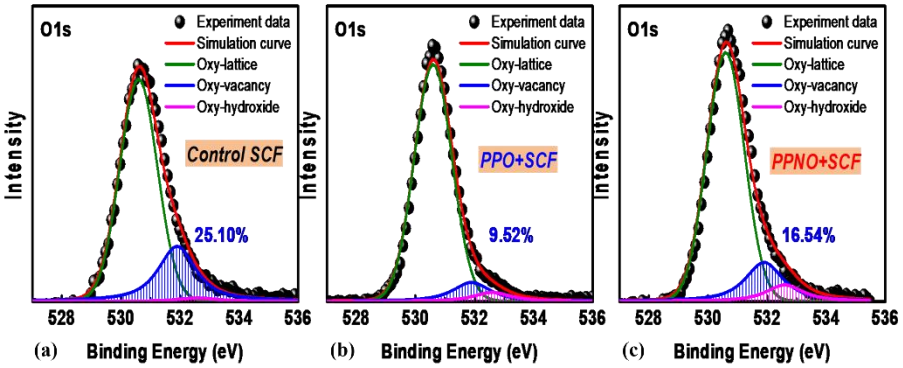

Fig. 2 XPS analysis of Ge sample (a) w/o, (b) with PPO+SCF, and (c) with PPNO+SCF treatment.

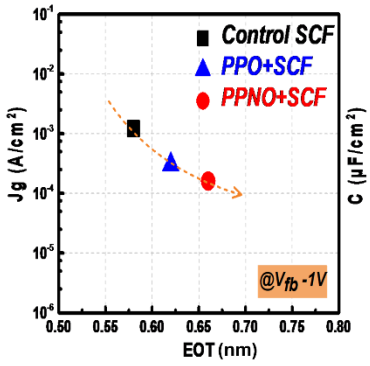

Fig. 3 Comparison of J_G-EOT with different treatments in this work.

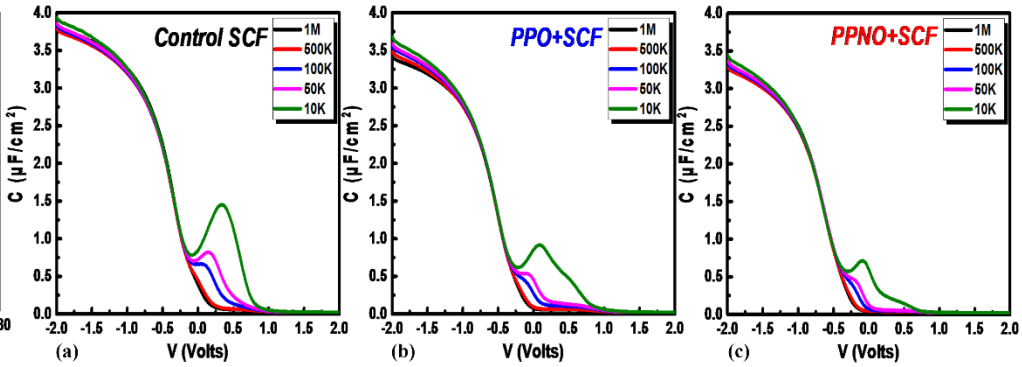

Fig. 4 The frequency dispersion of Ge nMOSCap (a) w/o, (b) with PPO+SCF, and (c) with PPNO+SCF treatment.

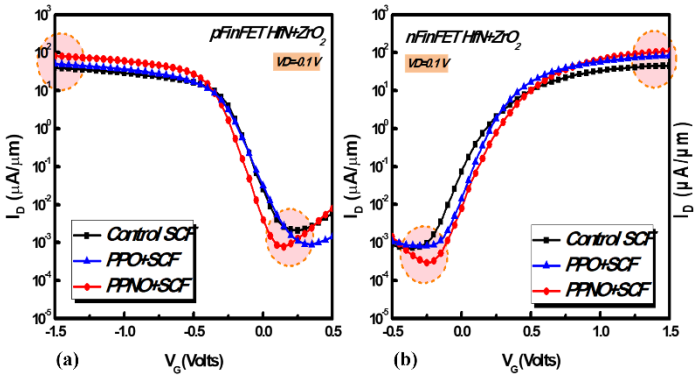

Fig. 5 The I_D-V_G curves for Ge (a) pFinFET and (b) nFinFET with different treatments in this work.

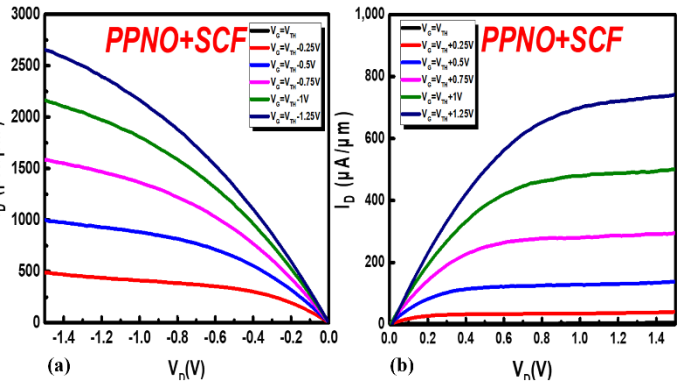

Fig. 6 The I_D-V_D curves for Ge (a) pFinFET and (b) nFinFET with PPNO+SCF treatment.

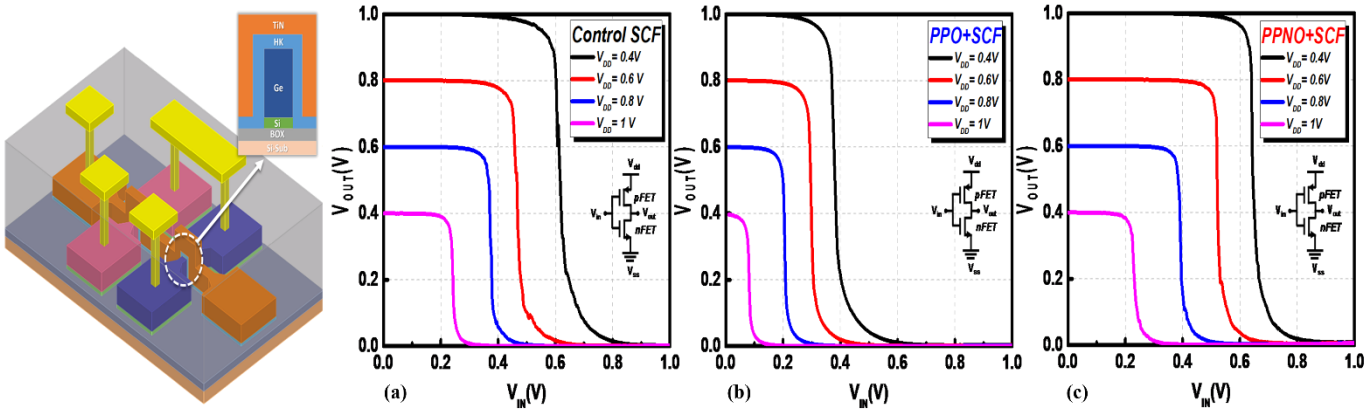

Fig. 7 V_{OUT}-V_{IN} curves for Ge FinFET CMOS inverter (a) w/o, (b) with PPO+SCF, and (c) with PPNO+SCF treatment.

Fabrication and Performance Analysis of Sol-Gel NiO/Si 830nm Near-Infrared Photodetectors Deposited by Spin-Coating Process

Yu-Xin Feng[1], Chien-Tso Lin[1], Jia-Hao Lin[2] , Yu-Hung Chen[1]
[1]Department of Microelectronics Engineering, National Kaohsiung University of Science and Technology, Kaohsiung City 811213, Taiwan
[2]Opto-Electronics Technology Section Energy and Agile System Department, Metal Industries Research & Development Centre, Kaohsiung, Taiwan
Email: yhchen@nkust.edu.tw

1. Introduction

Nickel oxide (NiO) due to its good optical transparency, wide bandgap properties (3.5 ~ 4.0 eV) [1] and the characteristics of N and P type semiconductor, in recent years special attention in the heterogeneous junction optoelectronic components.This study focuses on the preparation of NiO films on silicon substrates by low-temperature Sol-Gel Spin Coating method and its application to 830 nm near infrared (NIR) photodetectors.Under the optimized process conditions, the NiO films exhibited an 830 nm transmittance of 99.41% and an bandgap of 3.6 eV(see Fig.1), demonstrating excellent detection sensitivity and low dark current characteristics as near-infrared photodetectors.The effects of different annealing treatments on the structure and photoelectric properties of NiO films were also investigated to further evaluate the feasibility of using NiO/Si heterojunctions in near-infrared detectors.

2. Experimental Procedure

NiO_x solutions were spin coated on the cleaned Si substrate and the samples were heated at 200 ℃ for 15/30/40 min. By dissolving ethylene glycol, 1-butanol, and polyethylene glycol (PEG 600) in a beaker to prepare NiO_x solution. Next, nickel acetate ($Ni(CH_3COO)_2$) and ammonium hydroxide were added under magnetic stirring at room temperature for 30 min and then, stored at room temperature for 24 h. Finally, the Ni (100 nm)and Al (300 nm) electrodes were evaporated onto NiO_x and Si as ohmic contacts, respectively. (see Fig.2)

3. Results and Discussion

The p-type silicon substrate exhibits the best photoinductive performance under thickness of 180 nm and a 15 minute annealing condition, with a PDR of 776.7, a dark current of only 5.6×10^{-4} A, and a rectification ratio as high as 3607. With the extension of annealing time, the performance deteriorated sharply: when the annealing time was extended from 15 minutes to 30 minutes, the dark current rose to 6.5×10^{-3} A, and the PDR dropped to 252.6. If annealed for 40 minutes, the PDR drops to 68.4 and the dark current increases to 1.0×10^{-1} A.The results show that the NiO films on p-type silicon substrates are extremely sensitive to excessive annealing, and the interface quality deteriorates significantly with the prolongation of heat treatment time. In contrast, n-type silicon substrates show a completely opposite trend. When the annealing time was extended from 15 minutes to 30 minutes, the PDR increased significantly from 644 to 1.6×10^4. When further extended to 40 minutes, the PDR reached its peak value of 4.6×10^4, which was 71.7 times higher than that at 15 minutes. This indicates that the n-type silicon substrate achieves the best photoinductive performance only under 40 minute annealing conditions (PDR = 4.6×10^4, estimated dark current approximately 1.2×10^{-4} A). (see Fig.3)

I-V curve analysis shows that the series resistance and commutation ratio of p-type silicon substrate decrease with the increase of annealing time, and the interface quality deteriorates, which is consistent with the densification and carrier mobility decrease caused by excessive annealing of the film.On the other hand, the series resistance of n-type silicon substrate decreases (to 14.25 Ω at 30 minutes) and then slightly increases to 127.32 Ω at 40 minutes after moderately extending the annealing time, reflecting the complex process of interface reorganization and optimization.The UV-Vis-NIR measurement results of the film show its average transmittance at 830 nm is as high as 99.41%, and the band gap is 3.6 eV. The SEM results show that the longer the annealing time, the higher the density of the NiO film. (see Fig.4)

4. Conclusions

The NiO thin films prepared in this study exhibit a high average transmittance of 99.41% at 830 nm and a wide optical bandgap (3.6 eV), indicating excellent optical transparency. The annealing behavior of NiO with silicon substrates (p-Si and n-Si) shows that the NiO/p-Si device performs best with a short annealing time of

15 minutes, achieving a peak photo detection ratio (PDR) of 776.7 and a dark current of 5.6×10^{-4} A. In contrast, the NiO/n-Si device requires a longer annealing time of 40 minutes to reach optimal performance, with a PDR of 4.6×10^{4} and a dark current of 1.2×10^{-4} A, although its performance shows greater variability. SEM analysis indicates that the density of the NiO films increases with longer annealing times. Overall, adjusting the annealing conditions is crucial for improving the performance of NiO/Si heterojunction photodetectors, and the optimal parameters should be tailored based on the type of silicon substrate (p-type or n-type).

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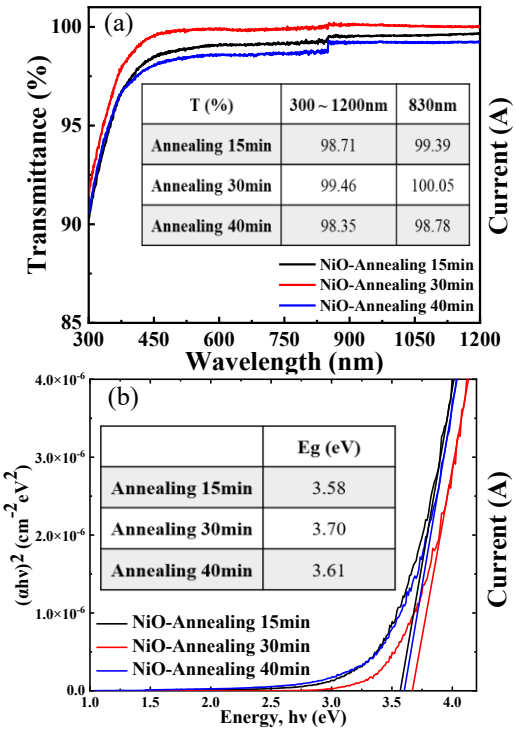

Fig. 1 These are the UV-Vis-NIR spectroscopic (a) transmittance. (b) bandgap under different annealing times.

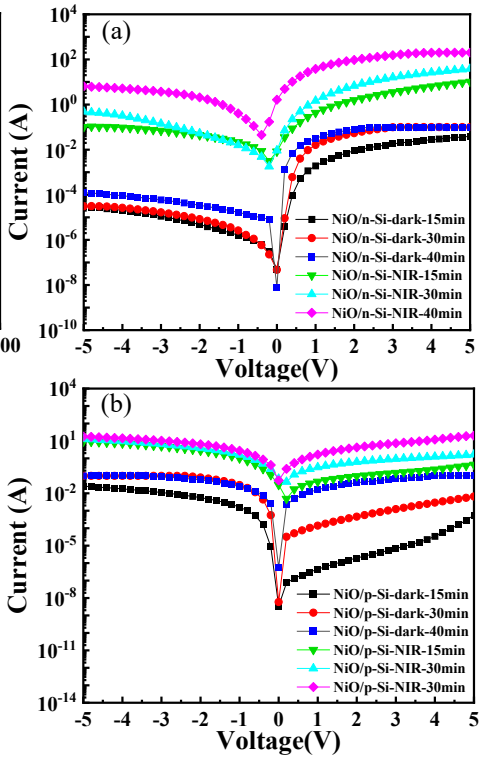

Fig. 3 (a) is the NIR and no light I-V characteristic of n-Si.(b) is the NIR and no light I-V characteristic of p-Si.

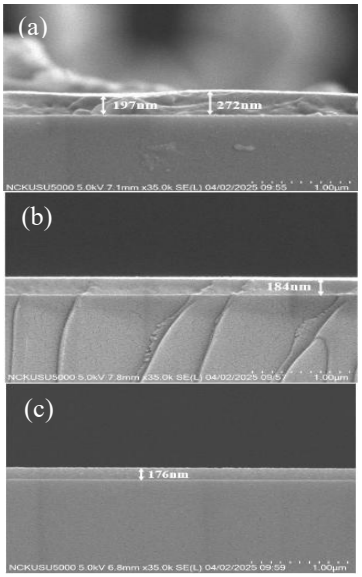

Fig. 4 SEM plots for different annealing times. (a) Annealing 15 mins, thickness 197nm. (b)Annealing 30 mins, thickness 184nm. (c)Annealing 40 mins, thickness 176nm.

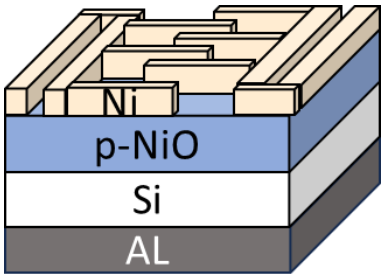

Fig. 2 Schematic diagram of NiO component.

New opportunity of GeSiSn/GeSn heterostructure for HEMT application

Shota Torimoto*[1], Mitsuo Sakashita[1], Masashi Kurosawa[1], Osamu Nakatsuka[1,2], and Shigehisa Shibayama[1]

[1]Graduate School of Engineering, Nagoya Univ., Furo-cho, Chikusa-ku, Nagoya, 464-8603, Japan
[2]IMaSS, Nagoya Univ., Furo-cho, Chikusa-ku, Nagoya, 464-8601, Japan

Tel: +81-52-789-2762, E-mail: s-shibayama@nagoya-u.jp

1. Introduction

High electron mobility transistor (HEMT) is one of attracted high-frequency operation devices under the terahertz technology. For HEMT composed of group-IV compounds, which is a low cost and nontoxic, there are reports about SiGe/Ge and Si/SiGe p-HEMTs [1,2]. Toward the further performance improvement of group-IV based p-HEMT, we focused on GeSn because GeSn can realize higher mobilities both electron and holes with increasing Sn composition compared to Si and Ge [3]. Furthermore, considering the heterostructure preferable to GeSn, GeSiSn/GeSn would be promising [4,5]. However, the examination of HEMT operation using GeSiSn/GeSn heterostructure has been lacked in both theoretical and experimental perspectives. Therefore, in this study, we addressed to clarify the application possibility of p-HEMT using GeSiSn/GeSn heterostructure from both directions of simulation and experiment.

2. Structural design by simulation

First, we examined the theoretical verification whether 2-dimensional hole gas (2DHG) can be formed at the GeSn surface by modulation doping of GeSiSn layer. For the simulation, we used nextnano software, where Schrodinger-Poisson equation was solved in the self-consistent method. Fig. 1(a) showed the structural model assumed in this simulation. The simulation parameter are the Si composition, x in $Ge_{0.95-x}Si_xSn_{0.05}$ layer and its thickness, W. Fig. 1(b) showed valence band edge structures of heavy and light holes, and the hole concentration distribution in the case of x and W of 0.3 and 20 nm, respectively. We found that quantum well and 2DHG are clearly formed at GeSn surface, suggesting that GeSiSn/GeSn p-HEMT can be realized. However, due to the presence of excess hole concentration in $Ge_{0.95-x}Si_xSn_{0.05}$ layer, for the numerical comparison, we estimated the hole area densities, S_{GeSiSn} and S_{GeSn} in $Ge_{0.95-x}Si_xSn_{0.05}$ layer and 2DHG region, respectively.

Fig. 1(c) summarized the S_{GeSn} ratio, r to the total hole area densities, $S_{GeSiSn}+S_{GeSn}$ as functions of x and W, where the 2DHG dominant condition is obvious by r closing to 1.0. We found that increasing x and thinning W can close r to 1.0. These directions would be reasonably understood because increasing x and thinning W lead to a deepened quantum well and an increased depletion region formed in $Ge_{0.95-x}Si_xSn_{0.05}$ layer, respectively.

3. Device fabrication and characterization

Based on the previous section, we examined the demonstration of GeSiSn/GeSn p-HEMT preparation and operation. An n-type Ge(001) substrate with a resistivity of 1.11–2.41 Ωcm was used as a substrate. After chemical cleaning and thermal treatment, 60-nm-thick undoped $Ge_{0.95}Sn_{0.05}$ and 20-nm-thick Ga-doped $Ge_{0.57}Si_{0.36}Sn_{0.07}$ layers were epitaxially grown in this sequence by molecular beam epitaxy at the substrate temperature of 150 °C. Pseudomorphic growth without any dislocations was verified by X-ray diffraction (XRD) and transmission electron microscopy (TEM) analyses (Figs. 2(a) and 2(b), respectively). Then, we performed the isolation and the formation of source/drain regions by photolithography and wet etching processes. Subsequently, we deposited a Al_2O_3 layer with a thickness of 25 nm by atomic layer deposition at 200 °C, opened contact holes by HF immersion, and formed Al gate/source/drain electrodes by the vacuum evaporation method. The cross-sectional structure and optical microscope image of p-HEMT prepared in this study were shown in Fig. 3(a).

Fig. 3(b) shows drain-current–drain-voltage, I_d–V_d characteristic measured at 10 K. We observed the transistor characteristics on the negative V_d side. Because $|I_d|$ tended to decrease with the increasing gate voltage, V_g, the HEMT showed a normally-on type operation as designed. However, as observed in I_d–V_g characteristic (Fig. 3(c)), I_d under off state was large and the further improvement to reduce an off current. According to the secondary ion mass spectroscopy (SIMS) analysis, we checked a Ga concentration in the $Ge_{0.57}Si_{0.36}Sn_{0.07}$ layer reaching ~10^{20} cm^{-3} order (Fig. 2(c)). This means that the prepared HEMT was under the excessive modulation doping condition. Considering simulation results of sheet hole densities of GeSn and GeSiSn layers depending on modulation doping concentration (*not shown here*), the leakage current owing to the current flowing in the $Ge_{0.57}Si_{0.36}Sn_{0.07}$ layer dominantly existed, possibly resulting in the degradation of the switching performance. Although some optimizations are needed to improve the device performance, the obtained results suggest that the GeSiSn/GeSn heterostructure can be applicated to p-HEMT as a new direction of the electrical application.

4. Conclusions

This study explored the possibility of GeSiSn/GeSn p-HEMT application by quantum mechanical simulation of energy band edge structure and carrier concentration distribution. Further, we experimentally demonstrated the normally-on transistor operation of GeSiSn/GeSn p-HEMT prepared in this study. Although the further improvement of the device performance is necessary, this study opened a new possibility the electrical application of GeSiSn/GeSn heterostructure.

Acknowledgments

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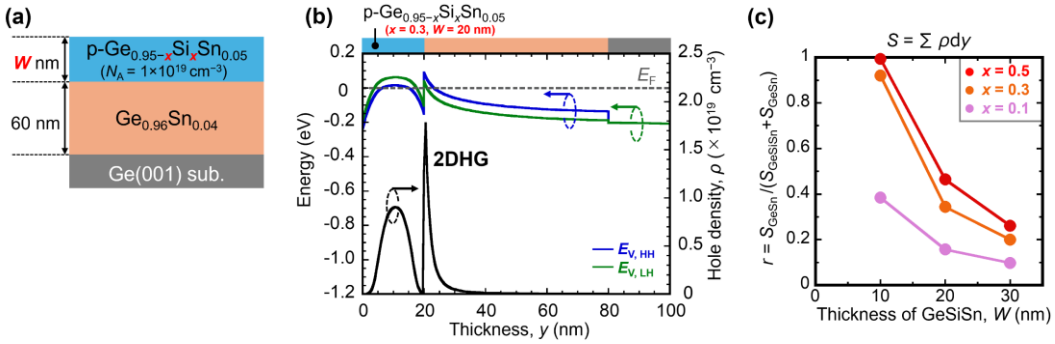

Figure 1 Quantum simulation of GeSiSn/GeSn heterostructure; (a) the schematic cross-sectional designed structure of GeSiSn/GeSn for simulation, (b) the valence band edge structures of heavy and light holes, and the hole concentration distribution at 300 K for x and W of 0.3 and 20 nm, respectively, and (c) the S_{GeSn} ratio to the total hole area densities, $S_{GeSiSn}+S_{GeSn}$ as functions of x and W.

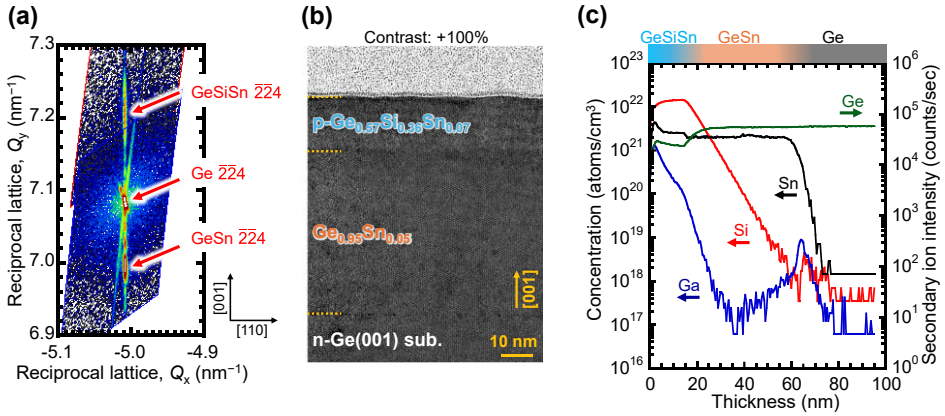

Figure 2 Crystal quality analysis of the epitaxial grown GeSiSn/GeSn heterostructure; (a) XRD-2DRSM, (b) cross-sectional HADDF-STEM image, and (c) SIMS profile for Ge, Si, Sn, and Ga.

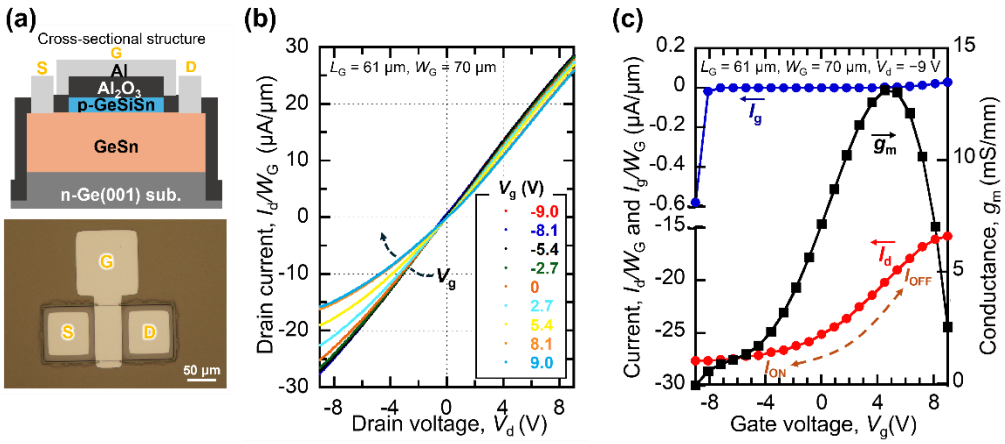

Figure 3 Fabricated GeSiSn/GeSn p-HEMT and its output characteristics; (a) the cross-sectional device structure and optical microscope images, (b) I_d−V_d curve measured at 10 K, and (c) I_d−V_g curve measured at 10 K.