Wed. Nov 5, 2025

Opening

📅 Wed. Nov 5, 2025 1:00 PM - 1:10 PM JST | Wed. Nov 5, 2025 4:00 AM - 4:10 AM UTC 🏛 5F-Meeting Room

[SO] Opening

Chair:Chihoko Kaneda(Tohoku University)

Keynote Address | Electron device, process, and characterization

📅 Wed. Nov 5, 2025 1:10 PM - 2:50 PM JST | Wed. Nov 5, 2025 4:10 AM - 5:50 AM UTC 🏛 5F-Meeting Room

[K] Keynote Address

Chair:Akinobu Teramoto(Hiroshima University), K.S. Chang-Liao(National Tsing Hua University)

1:10 PM - 2:00 PM JST | 4:10 AM - 5:00 AM UTC

[K-01]

Advanced Logic Transistor Innovation Towards "Beyond 2nm" Technology

*Toshiro Hiramoto[1], Hitoshi Wakabayashi[2] (1. The University of Tokyo (Japan), 2. Institute of Science Tokyo (Japan))

2:00 PM - 2:50 PM JST | 5:00 AM - 5:50 AM UTC

[K-02]

GaN Vertical Power Devices: Current Status and Future Prospects

*Jun Suda[1] (1. Nagoya University (Japan))

Hf-based Ferroelectrics | Electron device, process, and characterization

📅 Wed. Nov 5, 2025 3:10 PM - 5:20 PM JST | Wed. Nov 5, 2025 6:10 AM - 8:20 AM UTC 🏛 5F-Meeting Room

[S1] Hf-based Ferroelectrics

Chair:Reika Ichihara(KIOXIA), Yoshihumi Hiranaga(Tohoku University)

3:10 PM - 3:40 PM JST | 6:10 AM - 6:40 AM UTC

[S1-01]

Interface Engineering for Crystal Phase Control and High Fatigue Resistance in Ferroelectric HfO_2-Based Thin Films

*Takashi Onaya[1,2] (1. NIMS (Japan), 2. The Univ. of Tokyo (Japan))

3:40 PM - 4:00 PM JST | 6:40 AM - 7:00 AM UTC

[S1-02]

Impacts of oxidant selection and oxidant exposure time in ALD growth on crystallization of as-deposited HZO thin films

*Haoming Che[1], Takashi Onaya[1,2], Atsushi Tamura[1], Masaki Ishii[3], Hiroshi Taka[3], Koji Kita[1] (1. Dept. of Adv. Mater. Sci., The Univ. of Tokyo (Japan), 2. NIMS (Japan), 3. Taiyo Nippon Sanso (Japan))

4:00 PM - 4:20 PM JST | 7:00 AM - 7:20 AM UTC

[S1-03]

Growth and Ferroelectric Characterization of Lanthanoid-Doped Epitaxial HfO_2 Thin Films

Yutaro Tsuchiya[1], Kohei Shimonosono[1], Kazuki Okamoto[1], Wakiko Yamaoka[2], Yasunaga Kagaya[2], Yukari Inoue[2], *Hiroshi Funakubo[1] (1. Institute of Science Tokyo (Japan), 2. TDK Corporation (Japan))

4:20 PM - 4:40 PM JST | 7:20 AM - 7:40 AM UTC

[S1-04]

Process and Composition Engineering of Hafnium-Zirconium Oxide in MIM Capacitors with Morphotropic Phase Boundary Formation

*Hao-chun Yang[1], Kuei-Shu Chang-Liao[2], Dun-Bao Ruan[1], Cheng-Hsueh Wu[1] (1. National Tsing Hua Univ. (Taiwan), 2. Fuzhou Univ. (China))

4:40 PM - 5:00 PM JST | 7:40 AM - 8:00 AM UTC

[S1-05]

Engineering Al_2O_3 Doping Layers via Flash Lamp Annealing to Enhance Ferroelectricity in HfO_2 Thin Films

*Hideaki Tanimura[1,2], Tomoya Mifune[1], Yuma Ueno[2], Yusuke Tani[2], Hironori Fujisawa[1], Seiji Nakashima[1], Ai Isohashi Osaka[1], Shinichi Kato[2], Takumi Mikawa[2] (1. Univ. of Hyogo (Japan), 2. SCREEN Semiconductor Solutions (Japan))

5:00 PM - 5:20 PM JST | 8:00 AM - 8:20 AM UTC

[S1-06]

Device Design Trade-off in Silicon Junctionless Floating-Body FeFET

*Qiao Chu[1], Shinichi Takagi[1], Mitsuru Takenaka[1], Kasidit Toprasertpong[1] (1. The University of Tokyo (Japan))

Opening

📅 Wed. Nov 5, 2025 1:00 PM - 1:10 PM JST | Wed. Nov 5, 2025 4:00 AM - 4:10 AM UTC 🏛 5F-Meeting Room

[SO] Opening

Chair:Chihoko Kaneda(Tohoku University)

1:00 PM - 1:10 PM JST | 4:00 AM - 4:10 AM UTC

Opening Remarks

Keynote Address | Electron device, process, and characterization

📅 Wed. Nov 5, 2025 1:10 PM - 2:50 PM JST | Wed. Nov 5, 2025 4:10 AM - 5:50 AM UTC 🏛 5F-Meeting Room

[K] Keynote Address

Chair:Akinobu Teramoto(Hiroshima University), K.S. Chang-Liao(National Tsing Hua University)

1:10 PM - 2:00 PM JST | 4:10 AM - 5:00 AM UTC

[K-01]

Advanced Logic Transistor Innovation Towards "Beyond 2nm" Technology

*Toshiro Hiramoto[1], Hitoshi Wakabayashi[2] (1. The University of Tokyo (Japan), 2. Institute of Science Tokyo (Japan))

2:00 PM - 2:50 PM JST | 5:00 AM - 5:50 AM UTC

[K-02]

GaN Vertical Power Devices: Current Status and Future Prospects

*Jun Suda[1] (1. Nagoya University (Japan))

Advanced Logic Transistor Innovation Towards "Beyond 2nm" Technology

Toshiro Hiramoto[1,3] and Hitoshi Wakabayashi[2,3]

[1]The University of Tokyo, [2]Institute of Science Tokyo, [3]LSTC

Email: hiramoto@nano.iis.u-tokyo.ac.jp

1. Introduction

The rapid global advancement of AI is fundamentally supported by progress in semiconductor technology, particularly in advanced logic devices. As AI applications continue to expand, the demand for computing power has been growing exponentially, driving an urgent need for further innovation in semiconductor scaling and performance. Recognizing the strategic importance of semiconductors in the AI era, governments around the world have announced major investments in their domestic semiconductor industries. Japan has also launched a national initiative to strengthen its semiconductor capabilities. In 2022, Rapidus Corporation was established with the goal of mass-producing 2nm logic chips, and the Leading-edge Semiconductor Technology Center (LSTC) [1] was also founded to conduct research and development on "beyond 2nm" technologies. In this presentation, recent trends in logic semiconductor devices are reviewed, and the ongoing R&D activities at LSTC are introduced.

2. Histrical and Future Trend

Figure 1(a) [2] shows the historical and future trend of semiconductor logic technology nodes since 1980, plotted based on data from major international conferences and the IRDS roadmap [3]. It is remarkable that the nominal technology node has continued to shrink for more than 45 years, following an almost exponential pace of miniaturization. In 2024, TSMC presented its 2nm logic technology [4], and in 2025, Intel announced its 18A technology [5]. However, despite continued scaling, the rate of improvement in device speed and energy consumption has slowed compared with the past, mainly due to fundamental physical limitations and increasing parasitic effects, as illustrated in Figure 1(b). Moreover, the rise in chip power density, shown in Figure 1(c) [2], has become a critical concern, posing serious challenges for overall system performance and energy consumption.

3. Project for "Beyond 2nm"

To address these challenges, LSTC is conducting the NEDO project titled "Technology Development for Beyond 2nm and Short TAT Semiconductor Manufacturing." In this project, elemental process technologies for "beyond 2nm" devices with scalability toward the 1nm node and beyond are being developed, as summarized in Table 1. The main research topics include: Gate stack technology, aiming at CET scaling and Vth control, BEOL technology focusing on the development and reliability of new interconnect materials, and epitaxial growth technology for (110) substrates to enhance channel mobility and device performance.

4. Summary

LSTC was established for the development of "beyond 2nm" technologies. Main topics are the gate stack technology, BEOL, and the epitaxial growth technology.

References

[1] https://www.lstc.jp/.
[2] Data has been updated based on T. Hiramoto and H. Wakabayashi, IEEE Silicon Nanoelectronics Workshop, 2024.
[3] International Roadmap for Devices and Systems (IRDS), More Moore, 2024 Edision, https://irds.ieee.org/.
[4] H. C. Lin et al., IEDM, 2024.
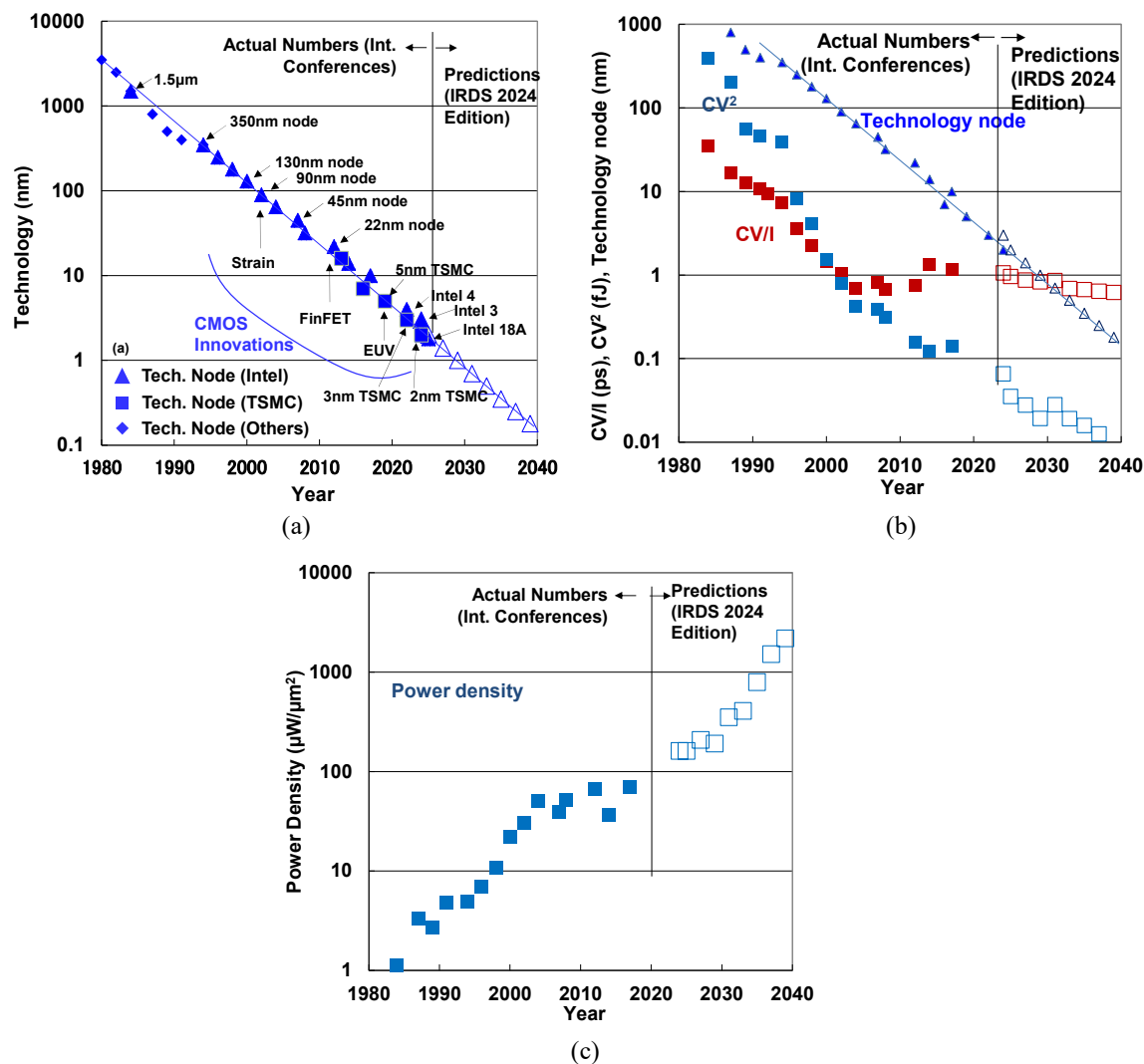[5] K. Fischer et al., VLSI, 2025.

Fig. 1. (a) Histerical and future trend of the technology node. (b) Trends of device delay time (CV/I) and energy (CV^2). (c) Trend of power density.

Table 1. Development items in "Technology Development for Beyond 2nm and Short TAT Semiconductor Manufacturing" in LSTC.

Items	Development focus
(1) Gate Stack	CET scaling, Vth control by dipoles and WF, Reliability.
(2) BEOL	New interconnect materials by MI, Reliability and Characterization of Post Cu interconnect.
(3) Epitaxial Growth	(110) substrate and epitaxial growth, Nanosheet formation, S/D epitaxial growth, Contact resistance.

GaN Vertical Power Devices: Current Status and Future Prospects

Jun Suda[1,2]

[1]Department of Electronics, Nagoya Univ., [2]IMaSS, Nagoya Univ.
[5]Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan
Email: suda.jun.t8@f.mail.nagoya-u.ac.jp / Phone: +81-52-559-9670

SiC and GaN have attracted much attention as semiconductor materials for next generation power devices. Thanks to large breakdown electric field, on-state (drift layer) resistance can be dramatically reduced to about 1/300 compared with that of Si. For SiC, vertical power devices such as SiC junction barrier Schottky (JBS) diodes, SiC double-implanted(DI)-MOSFETs and trench MOSFETs has been already commercialized. These devices are now used for train tractions, electric vehicles and power conditioners for renewable energy. These SiC devices are fabricated by using bulk SiC substrates.

On the other hand, development of GaN power devices had followed a different evolution path. Very high-density electron gas with high mobility was induced at $Al_xGa_{1-x}N$/GaN heterojunction. Combined with large breakdown field of GaN, high-power high-electron mobility transistors (HEMTs) can thus be realized. HEMTs are electron devices with lateral current path. In early days, large GaN bulk crystal was unavailable. Therefore, these devices must be fabricated on foreign substrates such as sapphire (Al_2O_3), Si or even SiC. Today, GaN-on-SiC HEMTs were widely used for microwave amplifiers due to its great high-power high-frequency performance (thanks to high-thermal conductivity and electrical insulating properties of SiC substrates). The GaN HEMT technologies were transferred for power switching devices. 600-V-class GaN-on-(low-cost)Si HEMT-based power switching devices have been commercialized over 10 years ago. Compact high-power AC power adaptors using GaN HEMTs have now become common.

GaN vertical power devices have also attracted much attention as next generation power devices with large current and high voltage capabilities (similar to SiC vertical power devices). Development of GaN bulk substrates with reduced dislocation density enables us to try fabrication of vertical power devices. Since GaN substrates were strongly required for mass production of GaN laser diodes (LDs). GaN bulk substrates became available since 2003. Pioneering works such as vertical AlGaN/GaN field-effect transistors or GaN trench MOSFETs on GaN substrates were presented in 2006. However, at that time, fundamental device processes for vertical devices, such as low-doped epitaxial growth, MOS, selective doping by ion implantation, were not established. Because of that, performance of these devices were not significant. However, for GaN bulk growth, melt or solution growth are possible in principle. There was a possibility of drastic reduction of wafer cost and increase of wafer size. It is very fascinating for power devices.

In 2014, U. S. ARPA-E started a new program, SWITCHES (strategies for wide bandgap, inexpensive transistors for controlling high-efficiency systems) including five vertical-GaN-power-device-related projects and four GaN-substrate-related projects. In the same year, Japanese government started a new project on "R&D of fundamental technologies for GaN vertical power devices (SIP-GaN)" as a part of cross-ministerial strategic innovation promotion program. Nine universities, five companies and one national laboratory joined the SIP-GaN project. The project focused on the most important fundamental technologies for GaN vertical power devices, i.e., bulk substrates, homoepitaxy of drift layers, ion implantation and MOS interface as well as characterization of fundamental material properties of GaN related to vertical power devices. Extensive investigations have been carried out. Later, Japanese government started a big GaN project, "Research and development of next-generation semiconductor to realize energy-saving society" covering crystal growth to device fabrications. These projects greatly advance R&D of GaN-on-GaN vertical power devices. And the project was followed by more power electronics oriented new program, "Innovative Power Electronics Technologies (INNOPEL)". In this paper, the author reviews recent progress and future challenges of GaN-on-GaN vertical power devices.

Table I Material parameters of various semiconductors.

	Si	GaAs	4H-SiC	GaN	β-Ga$_2$O$_3$	Diamond	AlN
Energy bang-gap (eV)	1.12	1.42	3.26	3.42	4.5	5.5	6.0
Electron mobility (cm^2/Vs)	1350	8000	1180	1480	200	4500	300
Electron saturation velocity (cm/s)	1×10^7	1×10^7	2×10^7	2×10^7	1.5×10^7	1.5×10^7	2×10^7
Breakdown field (MV/cm)	0.3	0.4	3	3	>7	>10	>10
Relative dielectric constant	11.8	13.1	10.3	10.4	10.2-12.4	5.7	8.5
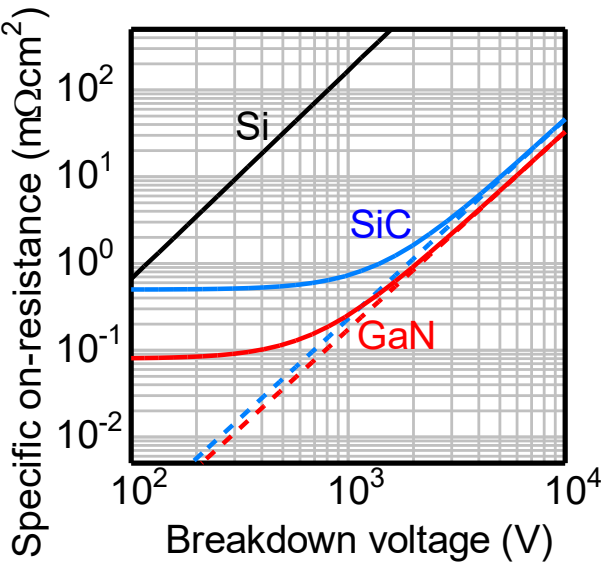
Fig. 1 Relationship between breakdown voltage and specific on-resistance of power MOSFETs. For high-voltage devices (>3 kV), the drift resistance (indicated by a dashed line) becomes dominant. In contrast, for lower-voltage devices (<2 kV), the dominant component is the channel resistance. Achieving high channel mobility is therefore essential for realizing ultra-low-loss devices. GaN is expected to exhibit such high channel mobility.

Hf-based Ferroelectrics | Electron device, process, and characterization

📅 Wed. Nov 5, 2025 3:10 PM - 5:20 PM JST | Wed. Nov 5, 2025 6:10 AM - 8:20 AM UTC 🏛 5F-Meeting Room

[S1] Hf-based Ferroelectrics

Chair:Reika Ichihara(KIOXIA), Yoshihumi Hiranaga(Tohoku University)

3:10 PM - 3:40 PM JST | 6:10 AM - 6:40 AM UTC

[S1-01]

Interface Engineering for Crystal Phase Control and High Fatigue Resistance in Ferroelectric HfO_2-Based Thin Films

*Takashi Onaya[1,2] (1. NIMS (Japan), 2. The Univ. of Tokyo (Japan))

3:40 PM - 4:00 PM JST | 6:40 AM - 7:00 AM UTC

[S1-02]

Impacts of oxidant selection and oxidant exposure time in ALD growth on crystallization of as-deposited HZO thin films

*Haoming Che[1], Takashi Onaya[1,2], Atsushi Tamura[1], Masaki Ishii[3], Hiroshi Taka[3], Koji Kita[1] (1. Dept. of Adv. Mater. Sci., The Univ. of Tokyo (Japan), 2. NIMS (Japan), 3. Taiyo Nippon Sanso (Japan))

4:00 PM - 4:20 PM JST | 7:00 AM - 7:20 AM UTC

[S1-03]

Growth and Ferroelectric Characterization of Lanthanoid-Doped Epitaxial HfO_2 Thin Films

Yutaro Tsuchiya[1], Kohei Shimonosono[1], Kazuki Okamoto[1], Wakiko Yamaoka[2], Yasunaga Kagaya[2], Yukari Inoue[2], *Hiroshi Funakubo[1] (1. Institute of Science Tokyo (Japan), 2. TDK Corporation (Japan))

4:20 PM - 4:40 PM JST | 7:20 AM - 7:40 AM UTC

[S1-04]

Process and Composition Engineering of Hafnium-Zirconium Oxide in MIM Capacitors with Morphotropic Phase Boundary Formation

*Hao-chun Yang[1], Kuei-Shu Chang-Liao[2], Dun-Bao Ruan[1], Cheng-Hsueh Wu[1] (1. National Tsing Hua Univ. (Taiwan), 2. Fuzhou Univ. (China))

4:40 PM - 5:00 PM JST | 7:40 AM - 8:00 AM UTC

[S1-05]

Engineering Al_2O_3 Doping Layers via Flash Lamp Annealing to Enhance Ferroelectricity in HfO_2 Thin Films

*Hideaki Tanimura[1,2], Tomoya Mifune[1], Yuma Ueno[2], Yusuke Tani[2], Hironori Fujisawa[1], Seiji Nakashima[1], Ai Isohashi Osaka[1], Shinichi Kato[2], Takumi Mikawa[2] (1. Univ. of Hyogo (Japan), 2. SCREEN Semiconductor Solutions (Japan))

5:00 PM - 5:20 PM JST | 8:00 AM - 8:20 AM UTC

[S1-06]

Device Design Trade-off in Silicon Junctionless Floating-Body FeFET

*Qiao Chu[1], Shinichi Takagi[1], Mitsuru Takenaka[1], Kasidit Toprasertpong[1] (1. The University of Tokyo (Japan))

Interface Engineering for Crystal Phase Control and High Fatigue Resistance in Ferroelectric HfO$_2$-Based Thin Films

Takashi Onaya[1,2]

[1] National Institute for Materials Science (NIMS), 1-1 Namiki, Tsukuba, Ibaraki 305-0044, Japan

[2] Dept. of Adv. Mater. Sci., The Univ. of Tokyo, 5-1-5 Kashiwanoha, Kashiwa, Chiba 277-8561, Japan

Email: ONAYA.Takashi@nims.go.jp / Phone: +81-29-860-4770

1. Introduction

Hf$_x$Zr$_{1-x}$O$_2$ (HZO) has been intensively studied among ferroelectric HfO$_2$-based materials because it exhibits ferroelectricity even with a wide range of Hf:Zr composition and at a low-temperature process below 400°C [1]. To achieve superior ferroelectricity in HZO thin films, it is required to form orthorhombic (O) phase, which is thought to be the ferroelectric phase [2]. In addition, the reliability of HZO-based ferroelectric devices should be considered for practical applications. The fatigue, which is degradation of switching polarization (P_{sw}) during repeated field cycling, is a critical reliability issue for HZO films, but the origin of fatigue remains unclear. In this study, we investigated interface reaction between the HZO film and TiN electrodes of TiN/HZO/TiN metal–ferroelectric–metal (MFM) capacitors during field cycling to clarify the origin of fatigue. We also demonstrated enhanced ferroelectric O phase formation and high fatigue resistance by designing the HZO/TiN interface.

2. Experimental Procedure

TiN/HZO/TiN MFM capacitors were fabricated as follows. A 10-nm-thick HZO film with the Hf/Zr ratio of 0.4/0.6 was deposited on the TiN bottom-electrode (BE-TiN) by atomic layer deposition (ALD) at 300°C. Next, post-deposition annealing was performed at 400°C for 1 min in N$_2$ atmosphere. Finally, TiN top-electrodes (TE-TiN) were fabricated. After applying switching cycles, TE-TiN was removed using wet etching process. Then, synchrotron hard X-ray photoelectron spectroscopy (HAXPES) with the X-ray energy of 8 keV was carried out to characterize the chemical states of Ti at the HZO/BE-TiN interface. To promote ferroelectric O phase formation and improve fatigue properties, HZO-based MFM capacitors were also fabricated with ZrO$_2$ nucleation layers (w/ ZrO$_2$-NL) which were inserted at the TE-TiN/HZO and HZO/BE-TiN interfaces.

3. Results and Discussion

Fig. 1 shows HAXPES Ti 1s spectra of the HZO/BE-TiN samples with different applied switching cycles. The endurance property of the MFM capacitor was also shown in the inset of Fig. 1. The switching cycles of 10^0, 10^4, and 10^8 were assigned to pristine, wake-up, and fatigue states, respectively. In the pristine state, TiO$_x$N$_y$ interfacial layer at the HZO/BE-TiN interface was found to be formed due to the annealing and ALD processes. In the wake-up state, the Ti 1s spectra was almost the same as that of the pristine state. Therefore, no interface reaction occurred at the HZO/BE-TiN interface during wake-up field cycling. These suggest that dominant factors for the wake-up could be domain depinning and phase transformation to the ferroelectric O phase in the HZO bulk region [3]. In the fatigue state, on the other hand, the higher peak intensity of the Ti-O component was observed compared to those of the pristine and wake-up states. Therefore, the surface oxidation of the BE-TiN should occur during field cycling in the fatigue state, indicating that oxygen atoms were supplied from the HZO film to the BE-TiN. Thus, we concluded that the fatigue was attributed to the domain pinning caused by the formation of additional oxygen vacancies (V$_O$) in the HZO film due to the interface reaction at the HZO/TiN during field cycling.

To achieve high fatigue resistance and superior ferroelectricity, we focused on inserting ZrO$_2$ nucleation layers (ZrO$_2$-NLs) at the HZO/TiN interfaces of TiN/HZO/TiN MFM capacitors. These ZrO$_2$-NLs are expected to promote the formation of the ferroelectric O phase [4] and prevent interface reactions. Fig. 2(a) shows the polarization–electric field (P–E) curves of the w/ ZrO$_2$-NL capacitor and that fabricated without ZrO$_2$-NLs (w/o). The w/ ZrO$_2$-NL capacitor showed 2.3 times higher remanent polarization ($2P_r = P_r^+ - P_r^-$) of 29 μC/cm^2 compared to that (12 μC/cm^2) of the w/o capacitor because of higher O, tetragonal (T), and cubic (C) phases ratio in the HZO film by using ZrO$_2$-NLs as shown in the Fig. 2(b) [4]. Fig. 3 shows the endurance properties of the w/o and w/ ZrO$_2$-NL capacitors. The w/ ZrO$_2$-NL capacitor exhibited higher P_{sw} than the w/o capacitor from the pristine to fatigue state as shown in the inset of Fig. 3 because the P_{sw} of the w/ ZrO$_2$-NL capacitor in the pristine state was much higher.

When comparing the decrease rate in P_{sw} from the end of wake-up field cycling ($\sim10^3$ cycles) to 10^8 cycles, a smaller degradation of switching polarization ($\sim33\%$) was obtained for the w/ ZrO$_2$-NL capacitor compared to that ($\sim52\%$) for the w/o capacitor [5]. These results indicated that ZrO$_2$-NLs inserted at the HZO/TiN interfaces could prevent the formation of additional V_O in HZO films during field cycling. Therefore, we found that the w/ ZrO$_2$-NL capacitor exhibited higher $2P_r$ and higher fatigue resistance than the w/o capacitor. We also demonstrated that the MFM capacitor with a surface-oxidized BE-TiN, which formed an oxygen-rich interfacial layer at the HZO/BE-TiN interface, exhibited superior fatigue properties compared to those fabricated without intentional oxidation of the BE-TiN (data not shown). Based on these experimental results, one of the ways to improve fatigue properties is inserting an interfacial oxide layer as a blocking layer of oxygen atom movement as shown in Fig. 4 [6].

4. Conclusions

We found that one of the origins of the fatigue properties could be the additional V_O formation in HZO films caused by the interface reaction at the HZO/TiN interface during field cycling. Therefore, it is important to prevent the oxygen atom movement between the HZO film and TiN electrode during field cycling to suppress the P_{sw} degradation. The MFM capacitor with ZrO$_2$-NLs inserted at the TE-TiN/HZO and HZO/BE-TiN showed higher $2P_r$ and higher fatigue resistance than the w/o capacitor. Based on these results, careful design of the interface between the HZO film and electrode is necessary for the practical application of HZO-based ferroelectric devices.

Acknowledgements

References

[1] J.-H. Kim et al., ACS Appl. Electron. Mater. **5**, 4726 (2023).
[2] X. Sang et al., Appl. Phys. Lett. **106**, 162905 (2015).
[3] M. Pešić et al., Adv. Funct. Mater. **26**, 4601 (2016).
[4] T. Onaya et al., APL Mater. **7**, 061107 (2019).
[5] T. Onaya, ECS Trans. **112**, 75 (2023).
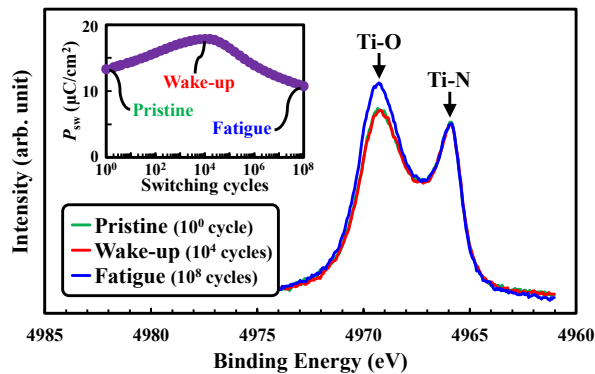[6] T. Onaya et al., Solid-State Electron. **210**, 108801 (2023).

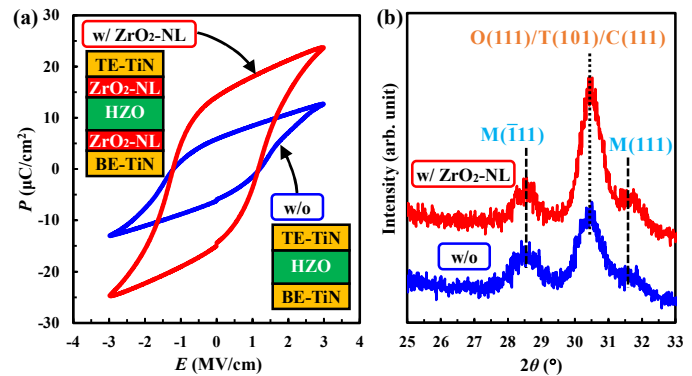Fig. 1 HAXPES Ti 1s spectra of the HZO/BE-TiN samples after applying different switching cycles.

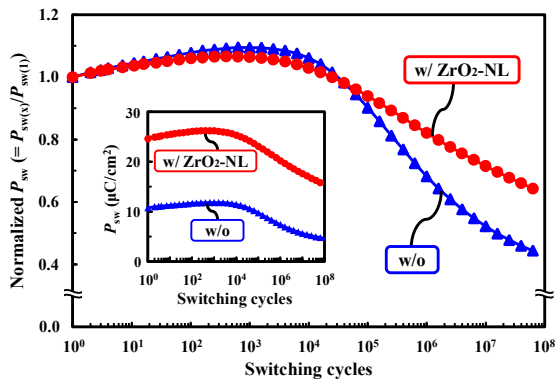Fig. 2 (a) P–E hysteresis curves and (b) GIXRD patterns of the w/o and w/ ZrO$_2$-NL MFM capacitors.

Fig. 3 Endurance properties of the w/o and w/ ZrO$_2$-NL MFM capacitors.

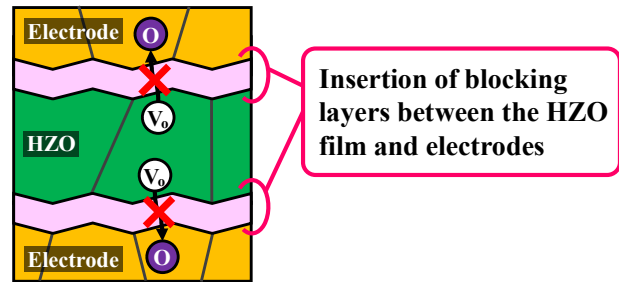
Fig. 4 Schematic of interface engineering for HZO based-MFM capacitors with high fatigue resistance.

Impacts of oxidant selection and oxidant exposure time in ALD growth on crystallization of as-deposited HZO thin films

Haoming Che[1], Takashi Onaya[1,2], Atsushi Tamura[1], Masaki Ishii[3], Hiroshi Taka[3], and Koji Kita[1]

[1]Dept. of Adv. Mater. Sci., The Univ. of Tokyo, [2]NIMS, [3]Taiyo Nippon Sanso,

[1]5-1-5 Kashiwanoha, Kashiwa-shi, Chiba 277-8561, Japan

Email: 3316270435@edu.k.u-tokyo.ac.jp / Phone: +81-4-7136-5456

1. Introduction

Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO), offering large remanent polarization at sub-10 nm thickness, can be precisely fabricated by atomic layer deposition (ALD) with excellent uniformity and step coverage. The ferroelectricity of HZO films originates from a metastable orthorhombic (O) phase [1]; thus, promoting O phase formation at low processing temperatures is critical for applications with strict thermal budgets, such as back-end-of-line (BEOL) integration at 400 °C or below. Residual impurities originated from incomplete reactions between precursor and oxidant during ALD are known to retard crystallization [2]. H_2O_2 is expected to be an ALD oxidant to reduce impurities more efficiently [3], owing to its higher oxidizing ability compared with conventional oxidant such as H_2O. Yet the influences of its exposure time per ALD cycle on impurity incorporation and crystallization of HZO film needs to be systematically investigated to clarify the advantage of employing it as ALD oxidant. Taking account of the previous report suggesting that partial crystallization in the as-deposited films is crucial to reduce the temperature to obtain fully crystallized films [4], this study examines as-deposited crystallization behavior and impurity level of HZO films grown by ALD using either H_2O or H_2O_2 with various oxidant exposure time.

2. Experimental Procedure

HZO/TiN/p-Si samples were fabricated as follows: 10-nm-thick HZO films were deposited on TiN (15 nm)/p-Si substrates by ALD at 250 °C using TEMAHf/Zr (Hf/Zr=1:1) as a precursor and either H_2O_2 or H_2O as an ALD oxidant, where precursor and oxidants were introduced by pulses as illustrated in Fig. 1. Exposure time of oxidants were varied by changing the number of oxidant pulses. H_2O_2 was vaporized with H_2O using N_2 as a carrier gas, by Peroxidizer®, RASIRC Inc. The concentration of H_2O_2 was determined to be ~5% by a concentration monitor (product of Ebara Jitsugyo Technologies). X-ray diffraction (XRD) was carried out to evaluate the crystallinities of as-deposited films. X-ray photoelectron spectroscopy (XPS) was used for impurity measurement.

3. Results and Discussion

Figure 2 shows XRD patterns of H_2O_2 and H_2O-based HZO films on TiN fabricated by various numbers of oxidant pulses. For all the films, a small diffraction peak appeared at $2\theta \approx 30.7°$, which was assigned to a mixture of component originates from the (111) plane of O, (101) plane of tetragonal (T), and (111) plane of cubic (C) phases, while there were no notable peaks originating from (-111) and (111) planes of the monoclinic (M) phase at $2\theta \approx$ 28.5° and 31.6°, indicating that as-deposited HZO films are dominantly crystallized into O/T/C phases. It is hard to deconvolute the peaks of O/T/C phases in XRD analysis using a laboratory-based X-ray source due to the very close peak positions of those phases.

Figure 3 illustrates the change of O/T/C phases peak area by the number of oxidant pulses employed in each ALD cycle for both oxidants. It can be observed that both H_2O_2 and H_2O-based HZO films showed a partial crystallization of O/T/C phases, while H_2O_2-based films always resulted in a larger peak area than H_2O-based films. Furthermore, with increasing the number of oxidant pulses, H_2O_2 and H_2O-based HZO films showed different trends in crystallization. For H_2O_2, when the number of pulses was five or more, the as-deposited crystallization was promoted and reached a saturation value. On the other hand, for H_2O, the crystallinity was not improved even by increasing the number of oxidant pulses up to seven. It was enhanced only when sufficient oxidation time (larger than 10 pulses/cycle) was provided and then gradually saturated. These results showed that the crystallization saturation rate of H_2O_2 is significantly higher than that of H_2O. Moreover, the distinct difference in crystallinity observed between the two oxidants indicates that the saturated crystallinity of H_2O-based films remains lower than that of H_2O_2-based films, even under conditions of excessive oxidation.

A possible explanation for the superior crystallinity achieved with H_2O_2 lies in its higher impurity removal efficiency. In this study, the impact of oxidation factors on residual impurities was systematically investigated, with impurity levels quantified by C 1s XPS analysis. After short-time Ar ion etching efficiently removed surface contaminants, the elemental composition remained stable irrespective of further etching. Two carbon species were

identified: one at 285 eV (attributable to C–C or C–H) and another at 286 eV (attributable to C–O or C–N). Carbon peak areas were normalized to Hf 4f peak, and it should be noted that the carbon signal originated from background was not eliminated in this analysis. As shown in Fig. 4, a decrease in the 285 eV carbon peak correlates with the O/T/C phases peak area (Fig. 4(a)), suggesting that this species may inhibits crystallization, whereas the 286 eV peak shows no clear relationship with crystallinity (Fig. 4(b)). In our previous study, Figure 5 of secondary ion mass spectrometry (SIMS) results clarified that not only residual carbon but also nitrogen levels of H_2O_2-based films were about one order of magnitude lower than H_2O-based films [5]. The nitrogen-to-carbon ratio was close to that of the precursor ligand, indicating that residual ligand fragments during ALD were the main source of impurities. Thus, using H_2O_2, a stronger oxidant, reduces precursor ligand components and related fragments in the film, simultaneously lowering carbon and nitrogen impurities and thereby enabling better as-deposited crystallization.

4. Conclusions

The crystallinity difference between the as-deposited HZO films with H_2O and H_2O_2-based ALDs was studied systematically. Extending the oxidation time can promote the crystallization of the film during the growth for both oxidants. H_2O_2-based ALD enables more effective removal of residual impurities during growth, leading to a higher as-deposited crystallinity compared with H_2O-based processes. H_2O_2-based films are expected to facilitate enhanced crystallization during subsequent low-temperature annealing.

References

[1] X. H. Sang et al., Appl. Phys. Lett **106**, 162905 (2015).
[2] H. S. Jung et al., J. Electrochem. Soc **159**, G33 (2012).
[3] Y. C. Jung et al., Appl. Phys. Lett **121**, 222901 (2022).
[4] T. Onaya et al., Microelectronic Eng **215**, 111013 (2019).
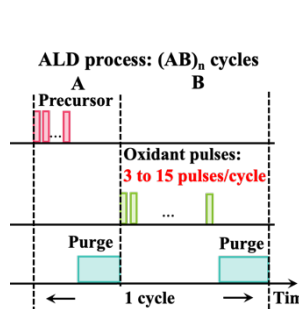[5] H. M. Che et al., Ext. Abst. Japan Society of Applied Physics Spring Meeting, Noda (2025).
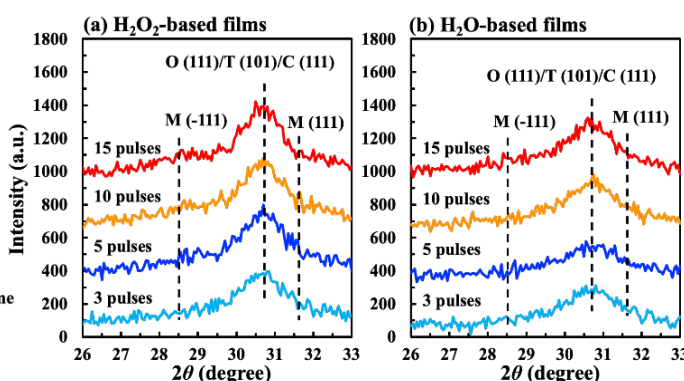
Fig. 1 Illustration of ALD cycles

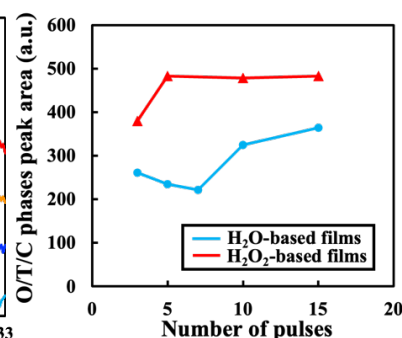Fig. 2 XRD patterns of (a)H_2O_2 and (b)H_2O-based HZO/TiN/p-Si samples fabricated by various numbers of oxidant pulses.

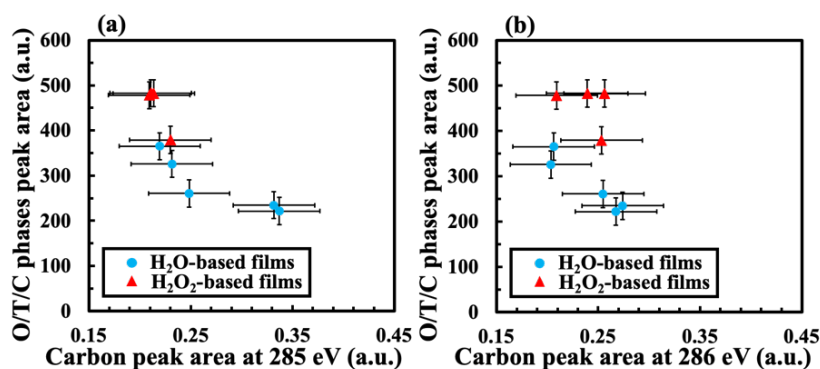Fig. 3 O/T/C phases peak area of H_2O and H_2O_2-based films with different number of oxidant pulses per ALD cycle.

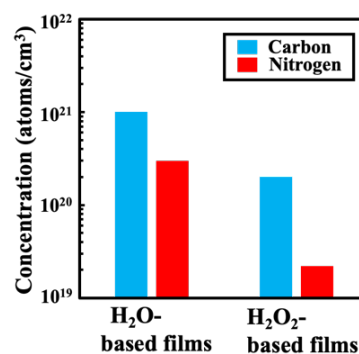Fig. 4 Relationship between O/T/C phases peak area of H_2O and H_2O_2-based films with carbon concentration.

Fig. 5 SIMS results [5] of carbon and nitrogen concentration of H_2O and H_2O_2-based films.

Growth and Ferroelectric Characterization of Lanthanoid-Doped Epitaxial HfO$_2$ Thin Films

Yutaro Tsuchiya[1], Kohei Shimonosono[1], Kazuki Okamoto[1], Wakiko Yamaoka[2], Yasunaga Kagaya[2], Yukari Inoue[2], and Hiroshi Funakubo[1]

[1]Science Tokyo., [2]TDK Corporation.,

[1]4259 Nagatsuta-cho, Midori-ku, Yokohama, Kanagawa 226-8501, Japan

Email: tsuchiya.y.2605@m.isct.ac.jp

1. Introduction

Since the first report of ferroelectricity in HfO$_2$-based thin films[1], this material system has attracted considerable attention for its use in next-generation nonvolatile memory applications. Doping with suitable elements is recognized to be particularly effective for the stabilizing ferroelectric orthorhombic phase. Although doping stabilizes the ferroelectric phase via combined changes in average ionic radius and oxygen vacancy formation, the indivisual effect of the average ionic radius on ferroelectric properties has remain unsolved.[2]-[4]

In this study, we investigate the effect of the average ionic radius of the cation on ferroelectricity. (111)-oriented epitaxial HfO$_2$-based films were grown, and trivalent lanthanoid elements with various ionic radius were doped with various contents.

2. Experimental Procedure

Lanthanoid–doped HfO$_2$ thin films (Ln^{3+}; La, Nd, Sm, Tm, Lu) with various contents were grown at room temperature on (111) ITO//(111) YSZ substrates by pulsed-laser deposition. Post-deposition heat treatment was performed by lamp annealing at 1000 °C for 10 min under an atmospheric N$_2$ gas flow. Crystal structure and film composition were evaluated by X-ray diffraction (XRD) and X-ray fluorescence (XRF), respectively. Circular Pt top electrodes were formed by electron-beam evaporation. Ferroelectric properties were evaluated by polarization–electric-field (P–E) measurements.

3. Results and Discussion

Figure 1 shows P–E hysteresis loops of xLnO$_{1.5}$–(1–x)HfO$_2$ (Ln = La, Nd, Sm, Tm, Lu) films as a function of dopant content. All dopants showed ferroelectricity for appropriate x values within the present study. Notably, dopants with larger ionic radius (*e.g.*, La) showed a broader composition window exhibiting ferroelectricity than those with smaller radius (*e.g.*, Lu). Figure 2 summarizes the dependence of the saturated polarization (P_{sat}) and coercive field (E_c) on the average cationic ionic radius estimated from the film compositions. P_{sat} monotonically increased with increasing average ionic radius. Based on the measured P_{sat} values, the spontaneous polarization (P_s) was estimated and shown in Figure 3(a). P_s increased from ~20 to ~40 μC cm^{-2} as the average ionic radius increased within 0.077–0.080 nm. We further estimated P_{sat} assuming random grain orientations from P_s value, and compared with the reported data for lanthanoid-doped HfO$_2$ (see Figure 3(b))[3],[5]-[10]. The estimated values almost agreed with reported ones and exhibit the same increasing trend with ionic radius, supporting the validity of our estimation.

4. Conclusions

Effect of the average ionic radius of trivalent lanthanoid dopants on the ferroelectric properties in epitaxial HfO$_2$ thin films was systematically investigated using well-defined (111)-oriented epitaxial films. Clear ferroelectricity was observed for films doped with all dopants. Saturation polarization (P_{sat}) and coercive field (E_c) almost proportionally increased with increasing average ionic radius as well as the estimated spontaneous polarization (P_s) value.

References

[1] T.S. Boscke *et al.*, Appl. Phys. Lett., 99, 102903 （2011). [2] J. Muller *et al.*, J. Appl. Phys., 110, 114113 (2011). [3] U. Schroeder *et al.*, Inorg. Chem., 57, 2752-2765 (2018). [4] F. Yan *et al.*, Mater. Horiz., 11, 626 (2024). [5] T. C. U. Tromm *et al.*, Appl. Phys. Lett., 111, 142904 (2017). [6] Z. Quan *et al.*, AIP Adv., 10, 085024 (2020). [7] S. Balahcen *et al.*, Appl. Phys. Lett., 117, 252903 (2020). [8] Y. Sharma *et al.*, Sol. Stat. Lett., 4, N13 (2015). [9] Y. Xiao *et al.*, IEEE Trans. Electron Devices 71, 6 (2024). [10] C. Mart *et al.*, Appl. Phys. Lett., 114, 102903 (2019).
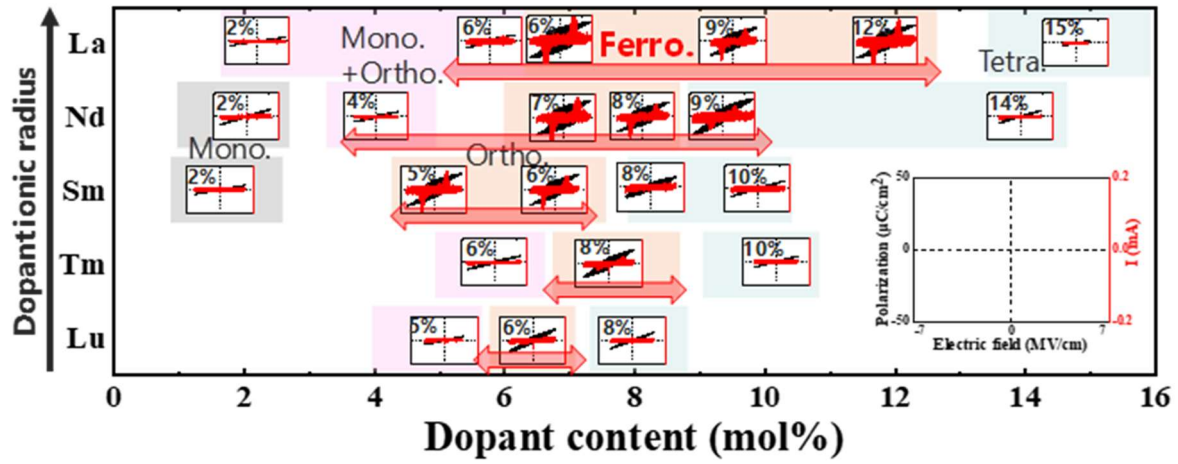
Fig. 1 *P-E* and *I-E* curves for xLnO$_{1.5}$–$(1-x)$HfO$_2$ thin films with various dopants a function of dopant content. Scale of the electric field, polarization and current are shown in the inset figure located at the right bottom edge.
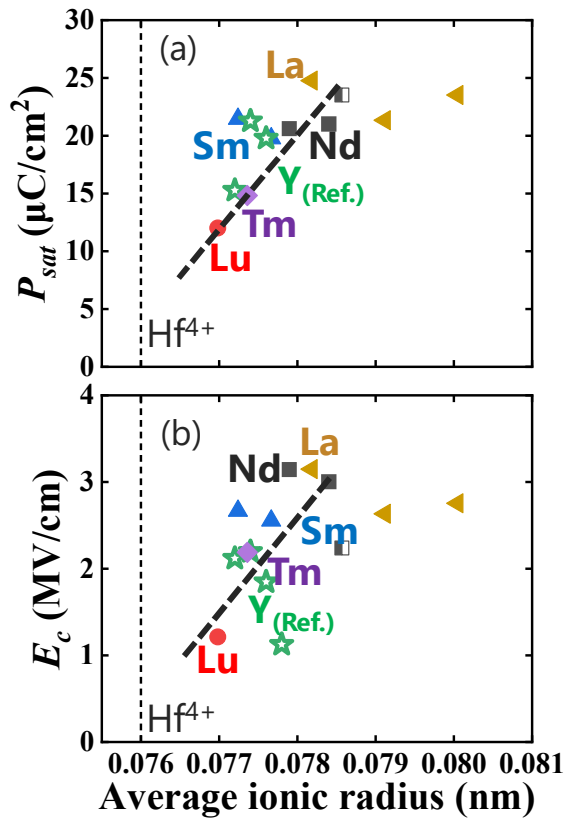
Fig. 2 (a) $P_{sat.}$ and (b) E_c as functions of the average ionic radius of xLnO$_{1.5}$–$(1-x)$HfO$_2$ thin films.
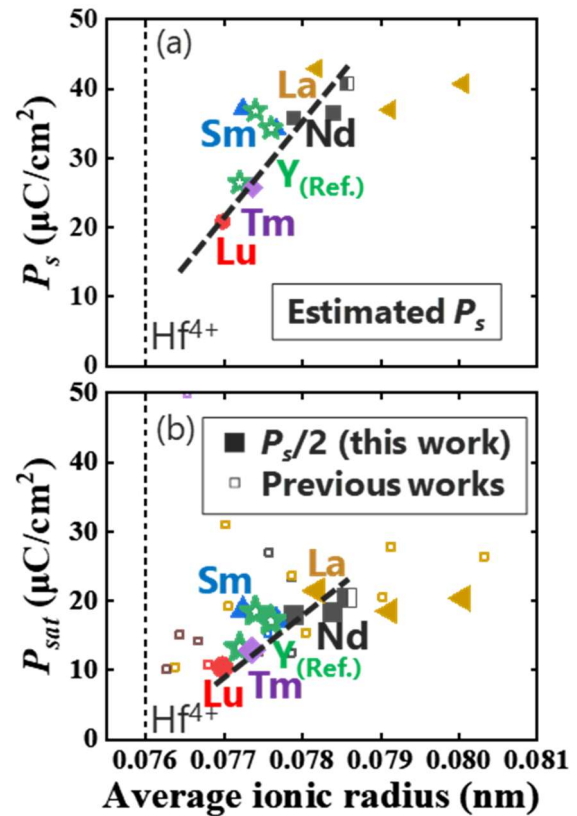
Fig. 3 (a) Estimated spontaneous polarization (P_s) and (b) expected saturation polarization ($P_{sat.}$) value assuming polycrystalline films ($P_s/2$) based on the estimated P_s value as a function of average ionic radius. Reported data for the lanthanoid-doped HfO$_2$ thin films are also shown in (b) as small open symbols.

Process and Composition Engineering of Hafnium-Zirconium Oxide in MIM Capacitors with Morphotropic Phase Boundary Formation

Hao-Chun Yang[1] , Dun-Bao Ruan[2] , Kuei-Shu Chang-Liao[1], and Cheng-Hsueh Wu[1]

[1]Department of Engineering and System Science, National Tsing Hua University, TAIWAN.

[2]College of Physics and Information Engineering, Fuzhou University, CHINA.

Email: jack1234567891040@gmail.com / Phone: +886-9-5205-1210

1. Introduction

As electronic devices shrink and diversify, the demand for high-density, low-leakage metal-insulator-metal (MIM) capacitors and tunable components like varactors has surged [1]. MIM capacitors are critical for decoupling capacitor, requiring high capacitance and thermal stability. Traditional SiO_2/Si_3N_4 dielectrics suffer from low dielectric constants (K), limiting capacitance density without thinning, which increases tunneling leakage [2]. Varactors, used in RF circuits for voltage-controlled capacitance, also require materials with tunable dielectric properties [3].

$Hf_{1-x}Zr_xO_2$ (HZO) thin films engineered to form a morphotropic phase boundary (MPB) between orthorhombic (o) and tetragonal (t) phases exhibit a high k value and enhanced ferroelectric polarization, ideal for MIM capacitors and varactors [4], [5]. For decoupling capacitor or DRAM, MPB enables high capacitance density and low leakage ($<10^{-7}$ A/cm²) with low EOT for efficient charge storage [4]. For varactors, MPB's C-V curves show significant capacitance variation with small voltage changes, enabling voltage-tunable capacitance for RF circuit applications [5], [6].

In this work, the film thickness, deposition temperature, PMA temperature, and Zr doping ratio of HZO on MPB formation in MIM capacitors were systematically investigated by assessing K value, EOT, leakage current density, and polarization performance.

2. Experimental Procedure

The MIM capacitors were fabricated on 6-inch Si wafers. After RCA cleaning, a ~5 nm SiO_2 layer was formed by rapid thermal oxidation (RTO). A 20 nm TiN bottom electrode was deposited via ALD, followed by an HZO dielectric layer deposited under various conditions with Zr:Hf ratios from 0.5 to 0.8. Three variables were investigated: dielectric thickness (7–13 nm at 250 °C), deposition temperature (200–300 °C at 9 nm), and PMA temperature (350–750 °C for 45 s in N_2). A 5 nm ALD-formed TiN capping layer and 50 nm PVD-formed top TiN electrode were added, followed by photolithography and dry etching to define the MIM structure.

3. Results and Discussion

A. Dielectric Thickness and Deposition Temperature

Thickness effects (7–13 nm) were studied at 250°C deposition and 550°C PMA. The K-V curves in **Fig. 1(a)** shows peak K near 0 V for MPB-like behavior, indicating increased dielectric constants with increasing thickness up to K=65.47 at 13 nm, suggesting improved crystallinity and reduced grain boundary defects. **Fig. 1(b)** shows the 13 nm sample exhibiting the lowest leakage (2.77×10^{-7} A/cm²), while the 9 nm sample achieves the thinnest EOT (0.7 nm) and acceptable leakage (3.22×10^{-7} A/cm² at 0.5 V). **Table I(a)** shows a thicker film can reduce leakage via fewer defects but increase EOT.

Deposition temperature (200–300°C) at 9 nm HZO plays a critical role on phase formation. In **Fig. 2(a), 2(b)** and **Table I(b)**, at 300°C, samples show the highest K (~60.9) and lowest EOT (0.59 nm), indicating better crystallinity and t-phase dominance, but with higher leakage (3.14×10^{-6} A/cm²) due to grain boundaries. The 200°C samples show the lowest leakage (2.87×10^{-7} A/cm²) but thicker EOT (0.81 nm). The optimal compromise is at 250°C, balancing capacitance and leakage through favorable crystalline ordering and reduced defect density.

B. PMA Temperature

PMA (350–750°C) at fixed 9nm/250°C HZO and [Zr/HZO]=75% is crucial in tuning stress via TiN-HZO thermal expansion mismatch to promote MPB formation. The K-V curve at 10 kHz in **Fig. 3(a)** show symmetric peaks; **Fig. 4(a), 4(b)** and **Table I(c)** show characteristics closest to ideal MPB with K=53.79 and EOT=0.68 nm by using a PMA at 650°C. P-V loops contracted at 650°C, confirming MPB. In **Fig. 3(b)**, leakage is minimized at 550°C (2.87×10^{-7} A/cm²).

C. Zr Doping Ratio

Zr ratios (50–80%) at 9nm/250°C/550°C PMA may alter bond lengths (Zr-O > Hf-O), inducing strain and different crystalline phases. The GIXRD in **Fig. 5** shows o-phase at 50–60%, transitioning to t-phase at >67%. **Fig. 6(a), 6(b), 7(a)** and **Table I(d)** show that a 60% Zr sample achievs the best performance (K=55.67, EOT=0.64 nm). In **Fig. 7(b)**, a 67% Zr sample is near to ideal MPB (K=51.27, EOT=0.7 nm). These align with Zr-O's longer bond inducing lattice strain for MPB facilitation.

4. Conclusions

It is found in this work that the process conditions and element content of HZO on electrical performance of MIM capacitors are strongly dependent on the formation of MPB mechaniam. By optimizing deposition parameters and Zr content, the formation of MPB phase could be enahnced, leading to high dielectric constants, reduced EOT, and controlled leakage current, which are crucial for high capacitance density MIM and varactor applications.

References

[1] K. Kim et al., in Proc. IEEE Int. Electron Devices Meet. (IEDM), 1.2.1 (2017).
[2] S. Mueller et al., Nano Lett. **12**, 4318 (2012).
[3] A. Victor et al., IEEE Trans. Microw. Theory Tech. **68**, 4657 (2020).
[4] J. Müller et al., in Proc. VLSI Technol., **25** (2012).
[5] T. S. Böscke et al., Appl. Phys. Lett. **99**, 102903 (2011).
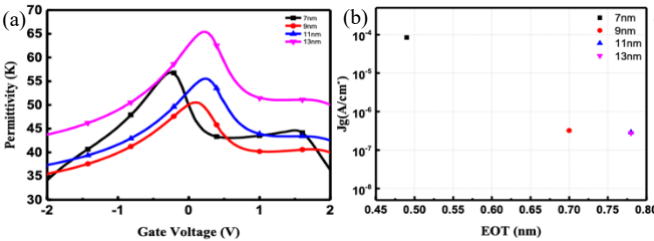[6] M. Dragoman et al., IEEE Electron Device Lett. **41**, 1345 (2020).

Fig. 1 (a) K-V (b) Jg-EOT characteristics of four dielectric layer thickness with 250°C deposition and 550°C PMA.
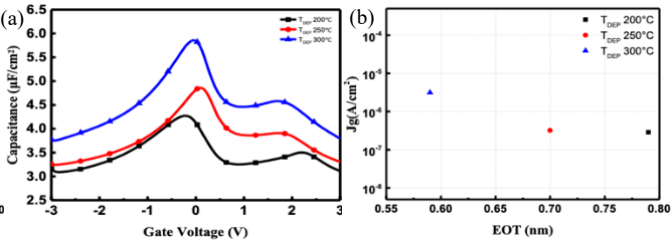

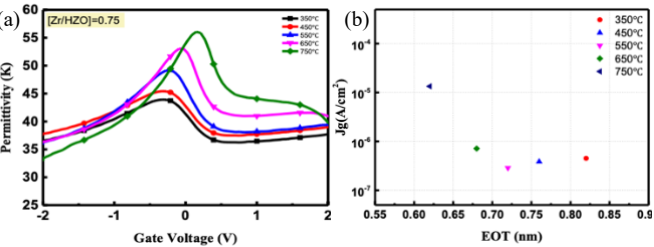Fig. 2 (a) C-V (b) Jg-EOT characteristics of three deposition temperature with 9nm 550°C PMA.

Fig. 3 (a) K-V (b) Jg-EOT characteristics of five PMA temperature with 9 nm/250°C HZO and [Zr/HZO]=75%.
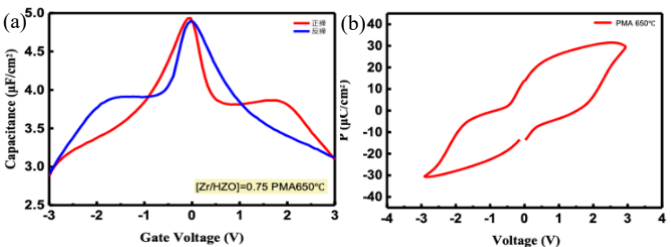

Fig. 4 (a) C-V (b) P-V curves of PMA 650°C with 9nm/250°C HZO and [Zr/HZO]=75%.
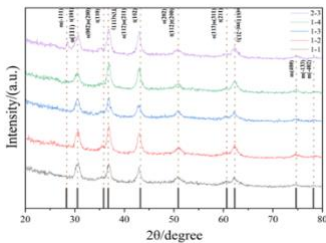

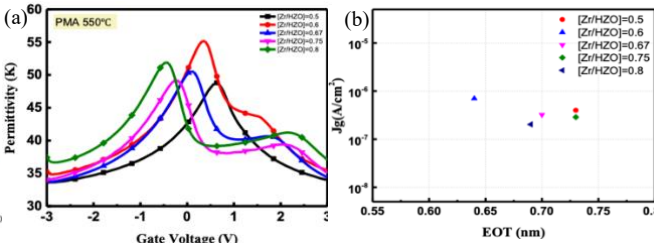
Fig. 5 GIXRD analysis of five Zr doping ratio.

Fig. 6 (a) K-V (b) Jg-EOT characteristics of five Zr doping ratio with 9nm/250°C and 550°C PMA.
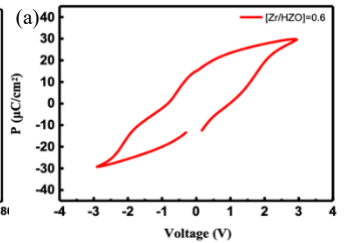

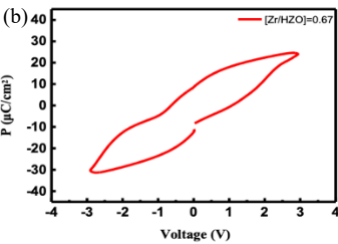Fig. 7 P-V curves of (a) 60% (b) 67% Zr doping ratio.

Table I K value and EOT of different (a) Dielectric thickness (b) Deposition temperature (c) PMA temperature (d) Zr doping ratio.

(a)

T_{DEP}	K	EOT
200°C	45.37	0.79
250°C	51.27	0.70
300°C	60.9	0.59

(b)

HK thickness	K	EOT
7nm	56.86	0.49
9nm	51.27	0.70
11nm	55.54	0.78
13nm	65.47	0.78

(c)

$Hf_{1-x}Zr_xO_2$	K	EOT
[Zr/HZO]=0.5	49.16	0.73
[Zr/HZO]=0.6	55.67	0.64
[Zr/HZO]=0.67	51.27	0.70
[Zr/HZO]=0.75	49.74	0.73
[Zr/HZO]=0.8	52.50	0.69

(d)

PMA	K	EOT
350°C	44.45	0.82
450°C	47.78	0.76
550°C	50.58	0.72
650°C	53.79	0.68
750°C	58.61	0.62

Engineering Al$_2$O$_3$ Doping Layers via Flash Lamp Annealing
to Enhance Ferroelectricity in HfO$_2$ Thin Films

Hideaki Tanimura[1,2], Tomoya Mifune[1], Yuma Ueno[2], Yusuke Tani[2], Hironori Fujisawa[1],

Seiji Nakashima[1], Ai I. Osaka[1], Shinichi Kato[2], and Takumi Mikawa[2]

[1]Univ. of Hyogo, [2]SCREEN Semiconductor Solutions

[1]Shosha 2167, Himeji, Hyogo 671-2280, Japan, [2]Takamiya-cho 480-1, Hikone, Shiga 522-0292, Japan

Email: tanimura@ screen.co.jp / Phone: +81-749-24-8460

1. Introduction

The doping of HfO$_2$ thin films is a widely adopted strategy to enhance their ferroelectric properties and improve phase stability. Among various approaches, aluminium-doped HfO$_2$ (HAO) has emerged as a promising candidate due to its superior characteristics which include a high remanent polarization value (2Pr) [1] and excellent thermal stability [2]. In this study, we demonstrate enhanced ferroelectricity in HAO thin films by retaining Al dopant position through a low-thermal-budget annealing method—millisecond-scale flash lamp annealing (FLA). We also revealed the dependence of the retained position of Al$_2$O$_3$ layers at the metal/ferroelectric interfaces on the polarization properties.

2. Experimental Procedure

Figure 1 presents a flow chart of the experimental procedure. A metal-ferroelectric-metal (MFM) capacitor structure was employed. For crystallization annealing, FLA was conducted with a duration of 5 ms at temperatures ranging from 800 to 1000 $^{\circ}$C. As a reference, rapid thermal annealing (RTA) was also performed for 60 seconds at temperatures between 400 and 700 $^{\circ}$C. Following annealing, transmission electron microscopy with energy-dispersive x-ray spectroscopy (TEM-EDX) was used to analyze the spatial distribution of Al within the HfO$_2$ films. Electrical measurements were undertaken after device patterning, using a triangular waveform with an amplitude of 6 V and a frequency of 10 kHz.

3. Results and Discussion

Figure 2 shows the Al distribution analyzed by TEM-EDX. The capacitor structure used in this study contains four Al layers, located at both the upper and lower interfaces, as illustrated in Fig. 2 (a). After FLA treatment, as shown in Fig. 2 (b), four distinct Al peaks are still observed even after high-temperature annealing at 1000 $^{\circ}$C. The peak positions closely match the initial structure prior to annealing, indicating that the doping layers are retained in their original positions thanks to the low-thermal-budget treatment. In contrast, Fig. 2 (c) presents the result of RTA performed at 600 $^{\circ}$C for 60 seconds. Although Al peaks are still observed, only three clear peaks are detected, despite the original structure containing four. This suggests that while retaining some Al dopants at their initial positions, significant redistribution occurs during RTA due to the longer annealing duration compared to millisecond-scale FLA.

The electrical performance was subsequently investigated, with a particular focus on the effect of the retained position of Al$_2$O$_3$ layers at the metal/ferroelectric interfaces. Two capacitor structures were prepared, as illustrated in Fig. 3: one with an Al$_2$O$_3$ retained layer at the top interface, and the other at the bottom interface. Two notable findings are observed in Fig. 3: (i) The top-retained Al$_2$O$_3$ layer positively influenced the 2Pr performance. For example, under FLA treatment, the 2Pr values were 36 and 31 μC/cm^2 for capacitors with the retained layer at top and bottom, respectively. Under RTA treatment, the difference was more pronounced: the 2Pr value for the top-retained layer was 29 μC/cm^2, whereas the bottom-retained layer exhibited insufficient ferroelectric response. (ii) FLA treatment yielded superior 2Pr performance compared to RTA, with values exceeding those of RTA by more than 20%. This improvement may be attributed to a greater tensile stress induced in the HAO film due to the lower thermal budget of the FLA treatment [3]. These results indicate that the combination of a top-retained layer and millisecond-scale FLA enhances the crystallization of HAO and increases the volume fraction of the ferroelectric orthorhombic phase.

4. Conclusions

Doping engineering with a top-retained layer enabled by FLA treatment is shown to be essential to enhance ferroelectric performance and is expected to contribute to the development of high-performance ferroelectric devices.

References

[1] B. Ku et al., Appl. Surf. Scie. **601**, 154039 (2022)
[2] G. Kim et al., pp. 106-109, IEDM (2022)
[3] H. Tanimura et al., Jpn. J. Appl. Phys. **63**, 09SP10 (2024).

- Cleaned p$^+$ Si (100) substrate
- Bottom TiN depo. (50 nm)
- HAO depo. (10 nm)
  - ALD: HfO$_2$ (TDMAH), Al$_2$O$_3$ (TMA)
  - Al conc. (=Al/(Al+Hf)): 3, 4 at%
- Top TiN depo. (50 nm)
- Patterning（Top TiN and HAO）
- Crystallization annealing
  - Rapid thermal annealing (RTA)
    Temp.: ~700 ^{o}C, time: 60 s
  - Flash lamp annealing (FLA)
    Temp.: ~1000 ^{o}C, time: 5 ms
- Evaluation
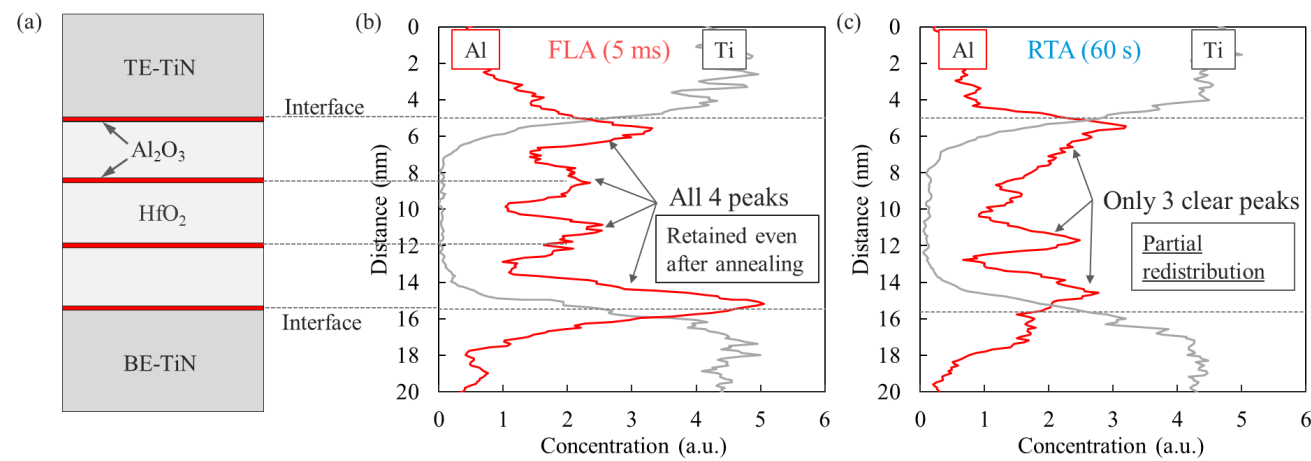 - TEM-EDX, P-E, GIXRD

Fig. 1 Experimental flow chart.

Fig. 2 (a) Illustration of the capacitor structure with four Al layers. Al distribution after (b) FLA treatment (5 ms at 1000 ^{o}C), and (c) RTA treatment (60 s at 600 ^{o}C). Al is retained even after annealing, particularly when using FLA.
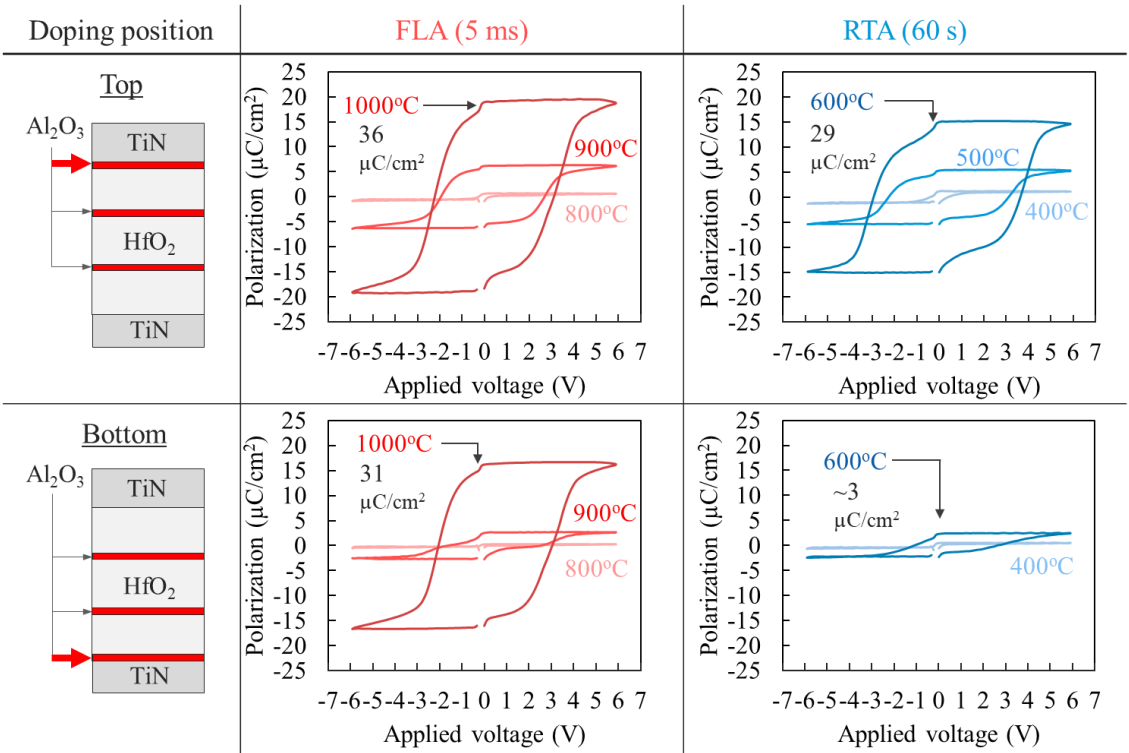

Fig 3. Effect of the doping position of the Al$_2$O$_3$ layer on electrical properties, measured using the positive-up-negative-down (PUND) method. The top-retained Al$_2$O$_3$ layer combined with FLA exhibits the highest 2Pr.

Device Design Trade-off in Silicon Junctionless Floating-Body FeFET

Qiao Chu[1], Shinichi Takagi[1], Mitsuru Takenaka[1], and Kasidit Toprasertpong[1]

[1]The Univ. of Tokyo

2-11-16 Yayoi, Bunkyo-ku, Tokyo 113-0032, Japan

Email: qiaoc@mosfet.t.u-tokyo.ac.jp

1. Introduction

Ferroelectric field-effect transistor (FeFET) has been drawing attention in recent decades since the discovery of HfO$_2$-based ferroelectric materials, mainly due to its CMOS compatibility and potential for high-density memory. While the memory properties of FeFET on bulk substrates have been widely studied [1], an understanding is still limited for FeFET with a thin floating body, which is currently taken into consideration when employed in scaled structures [2] and in 3D ferroelectric NAND [3]. In this work, we study the memory characteristics of floating-body FeFET through the TCAD simulation of junctionless silicon-on-insulator (SOI) FeFET, aiming to gain our understanding of the design trade-off between the memory window and cut-off characteristics.

2. Experimental Procedure

We explored the device characteristics of a junctionless SOI n-type FeFET with 10-nm HfZrO$_2$ (HZO) by TCAD simulation. The structure of investigated device is presented in Figure 1, with an 1-nm interfacial SiO$_2$ layer and gate work function (WF) as 4.6 V. The SOI is of uniform doping profile. The carrier transport was modelled by drift diffusion. The relative permittivity was $\varepsilon_r = 35$ for ferroelectric HZO. The remanent polarization was $P_r = 20$ μC/cm^2 and the coercive field was $E_C = 1.16$ MV/cm, respectively [3].

Quasi-static simulations were performed under a slow bidirectional gate voltage (V_g) sweep for 1000 s. $V_{th,avg}$ is defined as the center V_{th} of the two V_{th} states, where each V_{th} is defined by the constant current level of $W/L \times 10^{-7}$ A. Memory window (MW) is defined as MW $= \Delta E_C' \times T_{HZO}$, where $\Delta E_C'$ is the separation of the two effective coercive field in the polarization minor loop.

3. Results and Discussion

Figure 2 plots typical relationships between polarization and electric field under bidirectional sweep of $V_g = \pm 15$ V. As there is no hole contact in the junctionless floating-body structure, holes in channel were suppressed, resulting in a lack of positive charges to produce the sufficient electric field and switch polarization in HZO at negative V_g.

Figure 3 shows $V_{th,avg}$ with various combinations of doping concentration N_D and SOI channel thickness T_{SOI}. With higher N_D or thicker SOI, it is more difficult to turn off the channel. This can be seen in the severely negative value of the center threshold voltage. We further discuss the depletion region by depicting electron distribution in Figures 4(a) and 4(b) with different N_D and T_{SOI}. Under same negative gate bias, a device with lower N_D and thinner SOI is easier to fully deplete the channel.

The carrier distribution under different N_D and T_{SOI} leads to different electric field distribution, as shown in Figures 5(a) and 5(b). With higher N_D or thicker SOI in the channel, a large electric field in the ferroelectric layer would be easily produced at the negative gate voltage condition, resulting in a better polarization switching and an improved memory window as shown in Figure 6. Here, the relation with maximum depletion charge $Q_{dep} = qN_D T_{SOI}$ is also indicated in the plot as a common criterion. Whereas low N_D or thinner SOI is favourable to achieve a channel with better cut-off, the opposite is yet favourable to achieve better MW, implying that there exists the proper design space. From our result, it is observed that when Q_{dep} is smaller than 1 μC/cm^2, the MW is limited to as small as 1.1V; on the other hand, when Q_{dep} is larger than 2 μC/cm^2, the $V_{th,avg}$ rapidly shifts away from zero. We concluded that with N_D and T_{SOI} leading to Q_{dep} between 1 and 2 μC/cm^2, e.g., $N_D = 10^{19}$ cm^{-3} and $T_{SOI} = 10$ nm, both improved MW and reasonable cut-off can be obtained.

4. Conclusions

By TCAD simulation, we studied the memory window and threshold voltage in junctionless floating-body FeFET device. We described the impact of doping concentration and channel thickness on the cut-off behavior and the memory property and discussed the design space of such FeFET.

Acknowledgements

References
[1] K. Toprasertpong et al., IEEE Trans. Electron Devices **69**, 7113 (2022).
[2] W. Huang et al., IEEE Electron Device Lett. **43**, 25 (2022).
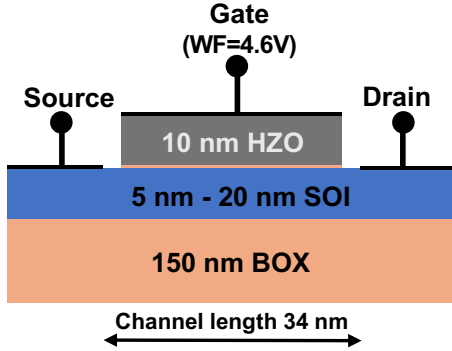[3] F. Mo et al., IEEE J. Electron Devices Soc. **8**, 717 (2020).
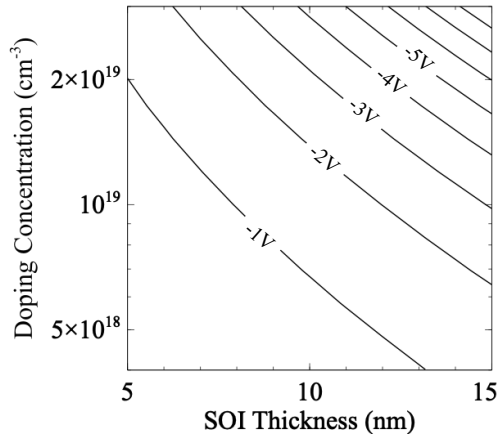

Fig. 1 Device structure of SOI FeFET.

Fig. 2 Polarization loop in proposed device.

Fig. 3 Center threshold voltage $V_{th,avg}$ in relation to N_D and SOI thickness.

Fig. 4 Electron distribution in the SOI channels of (a) T_{SOI}=5 nm and N_D=4×10^{18} cm^{-3} and (b) T_{SOI}=20 nm and N_D=4×10^{19} cm^{-3} under V_g=-10V, respectively. The depletion region edge is drawn with white solid line.

Fig. 5 Electric field distribution in the devices of (a) T_{SOI}=5 nm and N_D=4×10^{18} cm^{-3} and (b) T_{SOI}=15 nm and N_D=4×10^{19} cm^{-3} under V_g=-15V, respectively.
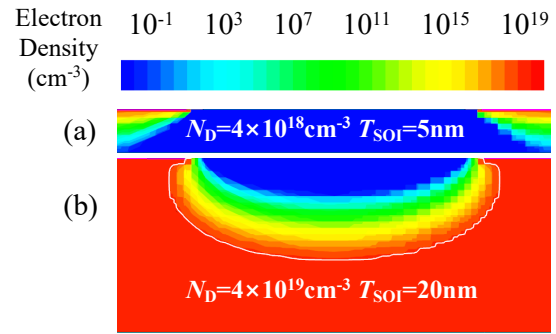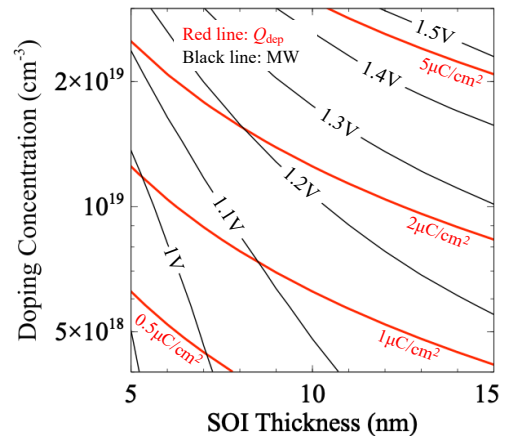

Fig. 6 Memory window MW (black line) and maximum induced charge Q_{dep} (red line) in relation to N_D and SOI thickness.