Fri. Nov 7, 2025

Thermal Oxidation Mechanism & 2D Materials | Simulation & Characterization

Fri. Nov 7, 2025 9:00 AM - 10:40 AM JST | Fri. Nov 7, 2025 12:00 AM - 1:40 AM UTC 5F-Meeting Room

[S5] Thermal Oxidation Mechanism & 2D Materials

Chair:Takanobu Watanabe(Waseda University), Koji Kita(The University of Tokyo)

9:00 AM - 9:20 AM JST | 12:00 AM - 12:20 AM UTC

[S5-01]

First-principles study of excess Si transport in Si oxide on Si substrate using two-layer-oxide model for thermally oxidized interface

*Hiroyuki Kageshima[1], Insung Seo[1], Toru Akiyama[2], Kenji Shiraishi[3] (1. Shimane University (Japan), 2. Mie University (Japan), 3. Tohoku University (Japan))

9:20 AM - 9:40 AM JST | 12:20 AM - 12:40 AM UTC

[S5-02]

Oxygen Pressure Dependence of Linear-Parabolic Growth Retardation on Si(111)

*Hengyu Wen[1], Yasutaka Tsuda[2], Yuki Okabe[1], Akitaka Yoshigoe[2], Jiayi Tang[3], Yuji Takakuwa[4], Shuichi Ogawa[1] (1. Nihon University (Japan), 2. JAEA (Japan), 3. JASRI (Japan), 4. Tohoku University (Japan))

9:40 AM - 10:00 AM JST | 12:40 AM - 1:00 AM UTC

[S5-03]

Cooperation Mechanism between Single- and Double-Step Oxidation Reaction Loops during Dry Oxidation on p-Si(001) and n-Si(001) Surfaces

*Yuki Okabe[1], Yasutaka Tsuda[2], Hengyu Wen[1], Akitaka Yoshigoe[2], Yuji Takakuwa[3], Shuichi Ogawa[1] (1. Nihon University (Japan), 2. JAEA (Japan), 3. Tohoku University (Japan))

10:00 AM - 10:20 AM JST | 1:00 AM - 1:20 AM UTC

[S5-04]

Segregation induced formation of two-dimensional like GeSn ultra-thin crystal

*Shigehisa Shibayama[1], Taiga Mtasumoto[1], Akio Ohta[2], Ryo Yokogawa[3,4,5], Mitsuo Sakashita[1], Masashi Kurosawa[1], Osamu Nakatsuka[1,6] (1. Grad. Sch. of Eng., Nagoya Univ. (Japan), 2. Faculty of Sci., Fukuoka Univ. (Japan), 3. RISE, Hiroshima Univ. (Japan), 4. Grad. Sch. of Adv. Sci. and Eng., Hiroshima Univ. (Japan), 5. MREL (Japan), 6. IMaSS, Nagoya Univ. (Japan))

10:20 AM - 10:40 AM JST | 1:20 AM - 1:40 AM UTC

[S5-05]

Role of Annealing Atmosphere Towards Stoichiometry and Chemical Integrity of Solution-Processed MoS_2 Thin films

*Md Iftekharul Alam[1], Shungo Nagata[1], Jaehyo Jang[2], Hayato Kosaka[1], Naoki Matsunaga[2], Yoshiteru Amemiya[1], Ryo Yokogawa[1], Hitoshi Wakabayashi[2], Akinobu Teramoto[1] (1. Hiroshima Uiversity (Japan), 2. Institute of Science Tokyo (Japan))

Focus Session | Electrically / Physicaly Characterization

Fri. Nov 7, 2025 10:55 AM - 11:55 AM JST | Fri. Nov 7, 2025 1:55 AM - 2:55 AM UTC 5F-Meeting Room

[FB] Focus Session B ~ Device Properties under Cryogenic Temperature

Chair:Akio Ohta(Fukuoka University), Takezo Mawaki(Tohoku University)

10:55 AM - 11:25 AM JST | 1:55 AM - 2:25 AM UTC

[FB-01]

(invite)Demonstration of Recovery Annealing on 7-Bits per Cell 3D Flash Memory at Cryogenic Operation for Bit Cost Scalability and Sustainability

*Yuta Aiba[1] (1. Frontier Technology Research & Development Institute., Kioxia Corporation (Japan))

11:25 AM - 11:55 AM JST | 2:25 AM - 2:55 AM UTC

[FB-02]

Toward Stable Operation of Si Quantum Computers: Origin of Long-period Charge Fluctuations in Si Fin-type Quantum Dots

*Hiroshi Oka[1], Hidehiro Asai[1], Kimihiko Kato[1], Takumi Inaba[1], Shota Iizuka[1], Yusuke Chiashi[1], Hitoshi Yui[1], Shoko Nagano[1], Shigenori Murakami[1], Yoshihisa Iba[1], Minoru Ogura[1], Takashi Nakayama[1], Hanpei Koike[1], Hiroshi Fuketa[1], Satoshi Moriyama[2], Takahiro Mori[1] (1. AIST (Japan), 2. Tokyo Denki Univ. (Japan))

Power Device & Processes | Electron device, process, and characterization

Fri. Nov 7, 2025 1:30 PM - 3:10 PM JST | Fri. Nov 7, 2025 4:30 AM - 6:10 AM UTC 5F-Meeting Room

[S6] Power Device & Processes (1)

Chair:Motoyuki Sato(Tokyo Electron), Toshinori Numata(Toyota Technological Institute)

1:30 PM - 2:00 PM JST | 4:30 AM - 5:00 AM UTC

[S6-01]

Carbon P_b centers in 4H-SiC/SiO_2 interface

*Takahide Umeda Umeda[1], Mitsuru Sometani[2], Bunta Shimabukuro[1], Yusuke Nishiya[3], Yu-ichiro Matsushita[3] (1. Univ. of Tsukuba (Japan), 2. AIST (Japan), 3. Quemix Inc./Tokyo Univ. (Japan))

2:00 PM - 2:20 PM JST | 5:00 AM - 5:20 AM UTC

[S6-02]

Study on Possible Origin of Improved 4H-SiC (0001) MOS Interface Characteristics with Direct NO Oxynitridation Based on Consideration of Oxinitride Growth Kinetics

*Yutaro Uchida[1], Atsushi Tamura[1], Koji Kita[1] (1. The Univ. of Tokyo (Japan))

2:20 PM - 2:40 PM JST | 5:20 AM - 5:40 AM UTC

[S6-03]

Impact of Substrate-Surface Oxidation Treatment and Post-Deposition Annealing on β-Ga_2O_3 (001) MOS Interfaces with ALD-Deposited Al_2O_3 and SiO_2

*Atsushi Tamura[1], Hayama Imaida[1], Hiroyasu Maekawa[2], Koji Kita[1,2] (1. Dept. of Advanced Materials Science, The Univ. of Tokyo (Japan), 2. Dept. of Materials Engineering, The Univ. of Tokyo (Japan))

2:40 PM - 3:10 PM JST | 5:40 AM - 6:10 AM UTC

[S6-04]

Exploration of new materials for meta-materials and power semiconductor applications

*Kentaro Kaneko[1] (1. Ritsumeikan Univ. (Japan))

Power Device & Processes | Electron device, process, and characterization

Fri. Nov 7, 2025 3:25 PM - 4:25 PM JST | Fri. Nov 7, 2025 6:25 AM - 7:25 AM UTC 5F-Meeting Room

[S7] Power Device & Processes (2)

Chair:Motoyuki Sato(Tokyo Electron), Toshinori Numata(Toyota Technological Institute)

3:25 PM - 3:55 PM JST | 6:25 AM - 6:55 AM UTC

[S7-01]

Effects of Nitrogen Doping on Electrical Properties of Ga_2O_3

*Masataka Higashiwaki[1,2], Jin Inajima[1], Tomoki Uehara[1], Yusuke Teramura[1], Kohki Tsujimoto[1], Satoko Honda[1], Zhenwei Wang[2] (1. Osaka Metropolitan Univ. (Japan), 2. National Institute of Information and Communications Technology (Japan))

3:55 PM - 4:25 PM JST | 6:55 AM - 7:25 AM UTC

[S7-02]

Unique techniques of ALD for semiconductor devices

*TOSHIHIDE NABATAME[1] (1. National Institute for Materials Science (Japan))

Closing

Fri. Nov 7, 2025 4:25 PM - 4:50 PM JST | Fri. Nov 7, 2025 7:25 AM - 7:50 AM UTC 5F-Meeting Room

[CS] Closing

Chair:Masao Inoue(Renesas Electronics), Mitsuru Sometani(National Institute of Advanced Industrial Science and Technology (AIST))

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Oxygen Pressure Dependence of Linear-Parabolic Growth Retardation on Si(111)

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First-principles study of excess Si transport in Si oxide on Si substrate using two-layer-oxide model for thermally oxidized interface

Hiroyuki Kageshima[1], Insung Seo[1], Toru Akiyama[2], and Kenji Shiraishi[3]
[1]Shimane Univ., [2]Mie Univ., [3]Tohoku Univ.
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1. Introduction

Silicon (Si) metal-oxide-semiconductor (MOS) interfaces are critical not only in conventional MOS field effect transistors (MOSFETs) but also in emerging Si-based devices, such as electron fluid effect devices and qubits for Si quantum computers. A detailed understanding of these interfaces is essential for further advancements in device performance. We have highlighted the significance of excess Si transport from the Si interface into the oxide layer during the thermal oxidation of Si. This excess Si transport is key to consistently explaining both the initially enhanced oxidation and the pattern-dependent oxidation. Furthermore, it provides a framework for understanding why the thickness and density of the interfacial high-density layer remain constant throughout the oxidation process, which is an essential factor in controlling interfacial reactions. We have investigated this excess Si transport by proposing that it occurs via SiO interstitials (I_{SiO}) [1-4]. In this study, we investigate excess Si transport at the thermal Si-oxide/Si interface from a broader perspective, using a two-layer-oxide model with cristobalite/quartz/Si interface, which effectively captures key characteristics of actual thermal oxide interfaces.

2. Method and Model

We investigate I_{SiO} transport paths in newly developed a two-layer-oxide model using first-principles calculations with PHASE0 [5]. The method details are similar to those in our previous studies [1-4]. The energy landscape is calculated based on the climbing-image nudged-elastic-band (CI-NEB) method.

The two-layer-oxide model with cristobalite/quartz/Si interface is constructed by stacking a cristobalite layer on top of our previously established quartz/Si interface model (Fig.1(a)). The model is simple yet sufficiently accurate to capture the averaged structural properties of the thermal Si oxide interface.

We have been using the quartz interface model because quartz can be formed by oxidizing Si-Si and then performing appropriate Si release for strain relaxation [6]. The quartz interface model was used to imitate this high density after the Si release as excess Si. We have shown that the quartz interface model must also be used to reproduce the barrier heights obtained experimentally for interfacial reaction process between oxygen (O_2) and Si [7]. The quartz layer at the interface must further keep a constant thickness regardless of the oxide thickness to reproduce the Deal-Grove theory. On the other hand, we have also shown that the cristobalite model must be used to reproduce the experimental barrier height for O_2 diffusion in the oxide film [8]. The density of the upper oxide layer is considered to be 2.2 g/cm^3 from various experiments, which is certainly consistent with the density of cristobalite. In other words, the Si thermal oxide film is considered to be

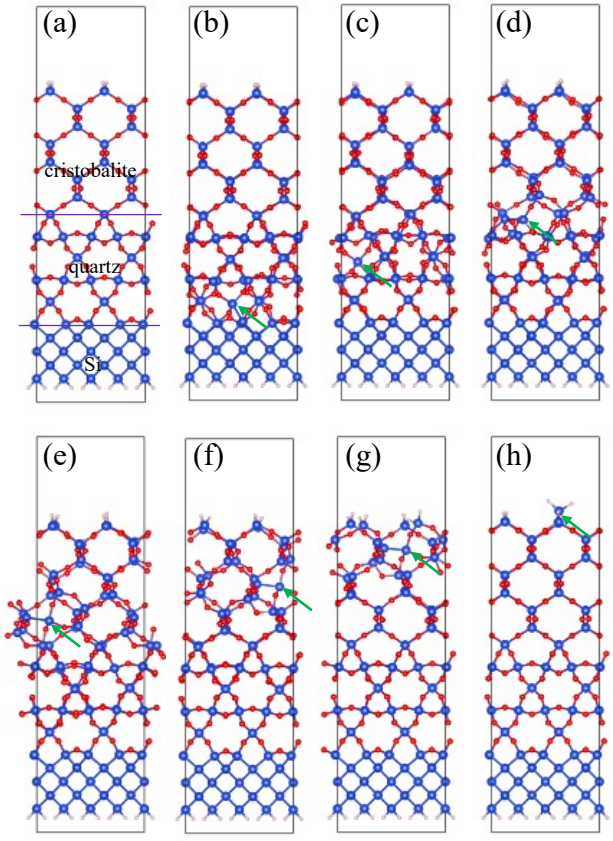

Fig. 1 (a) Atomic structure of the two-layer-oxide model with cristobalite/quartz/Si interface. And those of the metastable structures of I_{SiO} on the transport path: the (b) 0th, (c) 126th, (d) 186th, (e) 210th, (f) 234th, (g) 258th, and (h) 288th images corresponding to the horizontal axis in Fig. 2, respectively. Red and blue spheres indicate O and Si atoms, respectively. Green arrows indicate excess Si of I_{SiO}.

composed of at least two layers of oxide: a dense quartz-like interfacial layer and a cristobalite-like upper oxide layer.

Based on these considerations, we have successfully developed a model of the Si thermal oxide film interface. There are no dangling bonds anywhere and a seamless network of only Si-Si and Si-O-Si bonds without defects.

3. Results and Discussion

We have placed an I_{SiO} within the model, and successfully identified the transport path of the exess Si from the interface to the surface. The identified energy landscape is shown in Fig. 2, and some of metastable structures on the path are shown in Figs. 1(b)-(h). The indices of images correspond to the horizontal axis of Fig. 2.

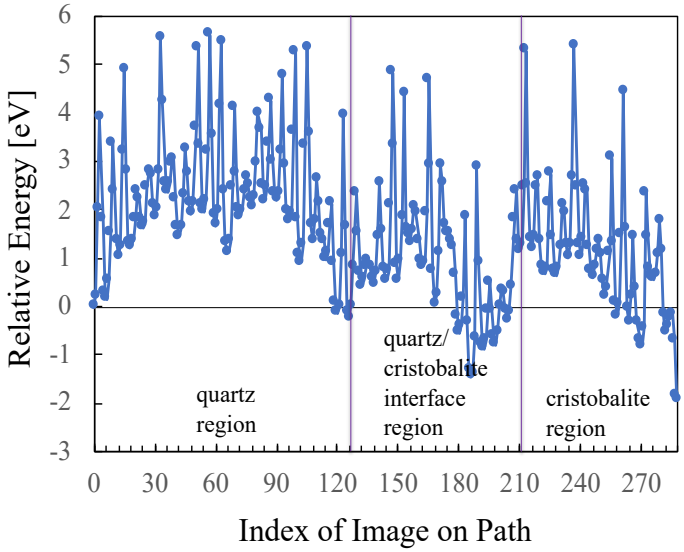

Fig. 2 Energy landscape for the transport path of I_{SiO} from the interface to the surface of the oxide in the two-layer-oxide model. The energies are measured from the 0th image.

The I_{SiO} is less stable by 1.12 eV at the 66th image in the middle of quartz layer than at the initial 0th image at the quartz/Si interface, and is also less stable by 0.70 eV at the 222nd image in the middle of cristobalite layer. However, it is slightly more stable by 0.23 eV at the 126th image at the surface of quartz layer, and even much more stable by 1.44 eV at the 186th image at the cristobalite/quartz interface. It further becomes significantly more stable by 1.92 eV at the final 288th image at the cristobalite surface. Notably, this surface stabilization is about 0.5 eV greater than that calculated at the quartz surface of the quartz/Si interface model in our previous study [4]. These results suggest that the excess Si can pile up at the cristobalite/quartz interface as well as at the cristobalite surface.

For the excess Si transport, the maximum barrier height through the quartz region (0th to 126th) is 5.61 eV, that through the cristobalite/quartz interface region (126th to 210th) is 4.84 eV, and that through the cristobalite region (210th to 288th) is 5.38 eV. Therefore, the overall barrier height is 5.61 eV. This value is larger than that of 4.55 eV calculated for the quartz/Si interface model in our previous study [4]. Because the surface is covered by the cristobalite layer, it seems that the quartz layer becomes less flexible and that the barrier height increases. However, this overall barrier height is still reasonably consistent with experimental results ranging from approximately 4 to 6 eV [9]. These results suggest that the excess Si can surely transport in the oxide from the interface to the surface during the Si thermal oxidation process.

4. Conclusions

We have constructed a two-layer-oxide model for the thermal Si oxide/Si interface, and successfully identified the excess Si transport path and its energy landscape in the oxide from the interface to the surface. We found that excess Si can pile up at the quartz/cristobalite interface as well as the cristobalite surface. We also found that the maximum barrier height is reasonably consistent with experiments.

Acknowledgements

A part of this study has been supported by KAKENHI (22K18294). A part of calculations is performed in the Super-computer Center of ISSP, University of Tokyo. Atomic structures are depicted with using VESTA.

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Oxygen Pressure Dependence of Linear-Parabolic Growth Retardation on Si(111)

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1. Introduction

The Si dry oxidation process is well described by the linear-parabolic growth model, except for the initial decrease in the oxidation rate below 20-40 nm [1]. Oxidation-induced vacancies act as O_2 dissociative adsorption sites during the initial decrease in oxidation rate [2-4]. According to this concept, single- and double-step oxidation reaction loops (Loops A and B) proceed cooperatively, and the reaction order of Loops A and B is first-order. Regarding the thickness of the SiO_2 layer, X_O, the linear-parabolic growth model is represented as follows:

$$X_O^2 + AX_O = B(t+\tau) \qquad (1)$$

In thin X_O, eq. (1) is approximated by eq. (2).

$$X_O \cong \frac{B}{A}(t+\tau) \qquad (2)$$

This means that the interfacial reaction is of zero order. This study investigates the origin of 0^{th}-order SiO_2 growth from the perspective of linear-parabolic growth retardation by observing X_O and ΔBB as a function of P_{O2} during dry oxidation on p-Si(111) surfaces with real-time XPS at SPring-8.

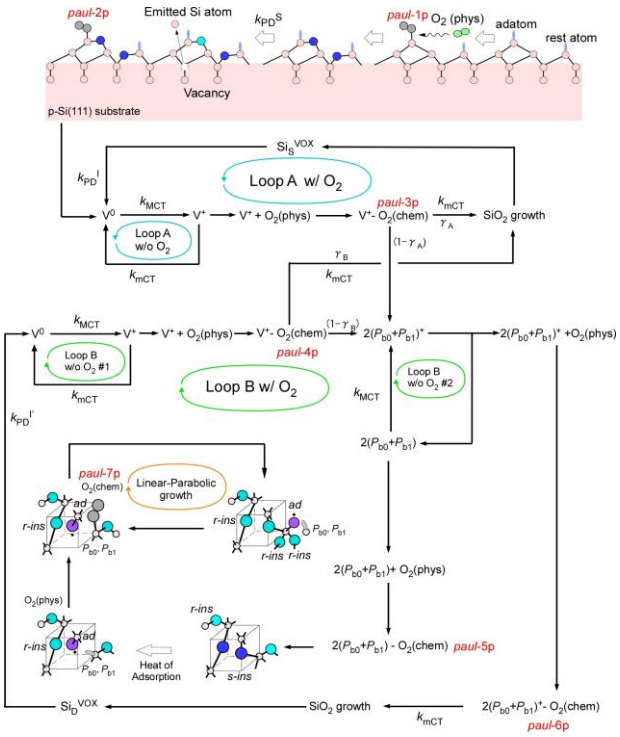

Fig. 1 Loops A/B & L-P model for p-Si(111) surface.

2. Loops A/B & L-P model

Figure 1 shows the Loops A/B and L-P model, in which the first-order reactions of Loops A and B are combined with the zero-order reaction of Loop L-P. In this model, X_O is represented as follows: A_A and A_B are the saturation levels, and k_A and k_B are the reaction coefficients for Loops A and B, respectively. A and B are the same as in Ref. [1]. For the retardation time of Loop L-P, $(t - \tau)$ is used in Eq. (3), which is different from Eq. (1).

$$Xo = A_A(1-e^{-k_A t}) + A_B(1-e^{-k_B t}) + \frac{1}{2}\left[-A + \sqrt{A^2 + 4B(t-\tau)}\right] \qquad (3)$$

The generation of point defects during surface oxidation marks the start of Loops A/B. The branching ratio between these loops is governed by γ_A, leading to the appearance of $2(P_{b0} + P_{b1})^+$. $2(P_{b0} + P_{b1})^+$ is the intermediate state of Loop B and the start of Loop L-P after minority carrier trapping. Oxidation-induced stress (about 8-11 gigapascals) and heat of adsorption (8-11 electronvolts) are responsible for the defect generation. There's a point defect (a missing atom) at the Si side in Loops A/B, and Si-O breaking ($Si_3 \equiv Si \cdot + \cdot O\text{-}Si \equiv O_3$) at the SiO_2 side in Loop L-P. $Si_3 \equiv Si \cdot$ can adsorb oxygen (O_2) and act as a P_{b0} center. However, for the vacancy site to be active, it needs to rearrange minority carriers.

3. Results and Discussion

As shown in Fig. 1(a), increasing P_{O2} has a big effect on enhancing silicon dioxide (SiO_2) growth. In the oxidation of Si(111) at 4×10^{-5} Pa, the surface oxidation process is best described by eq. (3) for only Loops A/B. The contribution from Loop L-P is not needed at all during the 1600-second time period examined, as shown in Fig. 1(b). Loop A takes about 2000 seconds, and SiO_2 growth continues through Loop B even at the end of

Oxidation I. As shown in Fig. 1(c), Oxidation II requires Loop L-P with an offset τ of 325 seconds, in addition to Loop B. dX_O/dt in Loop B increases 42 times, from 8.1×10^{-6} to 3.4×10^{-4} nm/s, upon an increase in P_{O2} from 4×10^{-5} to 4×10^{-3} Pa. It is important to note that τ in X_O is in good agreement with ΔE_k of Si^B, which quickly saturates and then increases gradually. Loop B is linked to a reduction in downward BB for p-Si, meaning a decrease in V^+. On the other hand, downward BB changes very gradually during Loop L-P. The latter supports the idea shown in Fig. 1. This figure shows that having extra minority carrier recombination is not necessary for the active site of $Si_3\equiv Si\cdot$ for O_2 dissociation in Loop L-P. However, majority carrier trapping ($V^0 + h^+ \rightarrow V^+$) plays an important role in activating the vacancy in Loops A/B.

When maintaining P_{O2} at 4×10^{-5} Pa, τ is extended to 4600 s (1600 s + 3000 s). This shows that L-P growth retardation is shortened from 3000 to 325 seconds by increasing P_{O2} 100 times at 500°C. When cooling down to room temperature at 4×10^{-5} Pa, τ is stretched to 6915s (1600s + 5315s). As a result, τ is shortened by raising the temperature and increasing P_{O2}. In Fig. 1, $2(P_{b0} + P_{b1})$-O_2^{2-}(chem), *paul*-5p, is the start of Loop L-P. *paul*-5p doesn't need minority carrier trapping for electric neutrality. However, hot hole trapping at the bonding orbital σ_g of O_2^{2-}(chem) makes it possible to dissociate O_2^{2-}(chem). The number of hot holes increases with rising temperature, according to the shortening of τ. On the other hand, hot holes are created through an Auger transition, which is associated with electron tunneling from Si CB to O_2(phys), resulting in O_2^-(phys). When $2(P_{b0} + P_{b1})$ and O_2^-(phys) hybridize, the result is the formation of *paul*-5p. Otherwise, electrons might tunnel from O_2^-(phys) to Si CB. The process of hopping at the interface causes the repetition of O_2(phys)⇄O_2^-(phys). This leads to the accumulation of enough hot holes. As P_{O2} increases, the hot hole accumulation becomes effective. This allows us to shorten τ, as we have observed. Additionally, Loop B without O_2 #2 makes the density of $2(P_{b0} + P_{b1})$ much smaller compared to that of $2(P_{b0} + P_{b1})^-$ in Loop B. This reduces the frequency of the formation of *paul*-5p a lot.

Once the Si-O bond is broken due to heat of adsorption ($Si_3\equiv Si\cdot$ + $\cdot$ O-Si$\equiv O_3$), an active site such as a P_{b0} center appears. This process is called "Si-O breaking", making it possible to start a process called "Loop L-P." The Si-O breaking number is more than one because of the sufficient heat of adsorption. The reason is that four Si-O bonds are formed by O_2 dissociation at the P_{b0} center and one Si-O is added due to rebonding between $Si_3\equiv Si\cdot$ and $\cdot$O-Si$\equiv O_3$. This means that Loop L-P is not limited by the number of $Si_3\equiv Si\cdot$ sites. Instead, it is governed by the supply of O_2^-(phys). This suggests that the 0^{th}-order reaction of Loop L-P is governed by O_2^-(phys). In Fig. 2, τ^{-1} and B/A show a nonlinear dependence on P_{O2}. Both of them are likely worried about the separation of O_2^{2-}(chem) because of hot hole trapping.

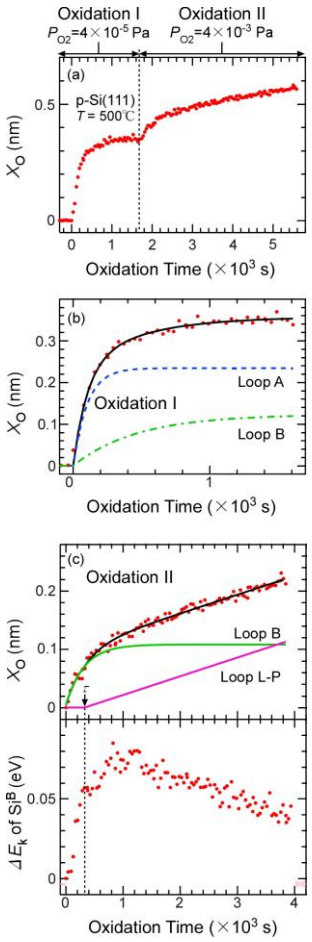

Fig. 2 (a) Changes of X_O upon P_{O2} increase between Oxidation I and II. Curve-fitting analysis of X_O: (b) Oxidation I and (c) II. (d) ΔBB obtained in Oxidation II.

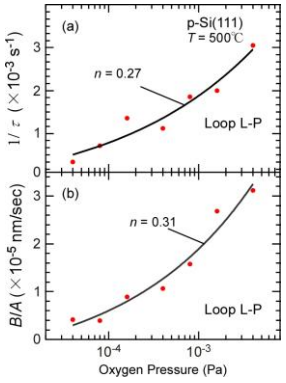

Fig. 3 P_{O2} dependence of (a) τ^{-1} and (b) B/A for Loop L-P.

4. Conclusions

The L-P growth retardation revealed the following: The origin of Loop L-P is $2(P_{b0} + P_{b1})^-$ in Loop B; The frequency of appearance of *paul*-5p is reduced by excess minority carrier recombination without O_2; The dissociation of *paul*-5p is governed by hot hole trapping; and Si-O breaking ($Si_3\equiv Si\cdot$ + $\cdot$ O-Si$\equiv O_3$) acts as an O_2 dissociation site.

References

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Cooperation Mechanism between Single- and Double-Step Oxidation Reaction Loops during Dry Oxidation on p-Si(001) and n-Si(001) Surfaces

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1. Introduction

The initial oxidation rate reduction in Si dry oxidation was interpreted by a unified Si oxidation reaction model mediated by oxidation-induced defect generation (Loops A/B & L-P model). In this model, single- and double-step oxidation reaction loops A and B are cooperated. Furthermore, majority and minority carrier trapping occur at vacancy-derived levels [2], and trapping-mediated adsorption of O_2 proceeds at vacancies and P_b centers [3]. In this study, the cooperative mechanism between Loops A and B was investigated by comparing SiO_2 thickness, X_O, between p-Si(001) and n-Si(001) surfaces. This was observed *in situ* as a function of temperature by XPS at SPring-8.

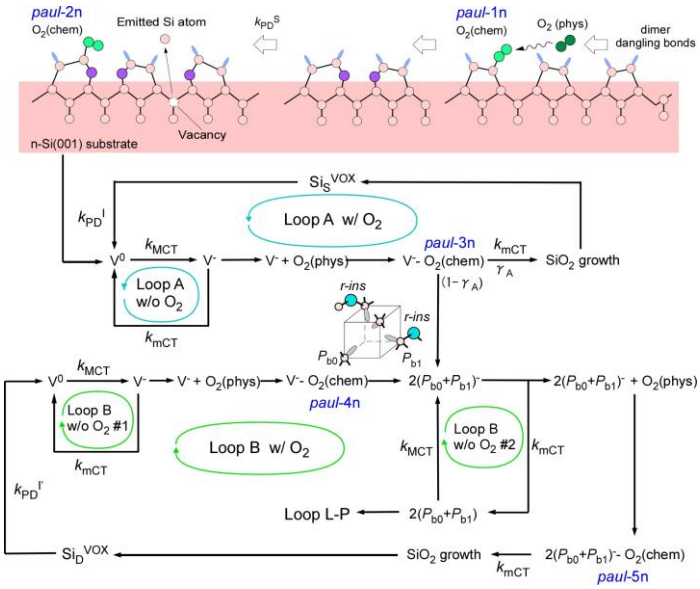

Fig. 1 Unified Si oxidation reaction model mediated by oxidation-induced point defect generation.

2. Loops A/B & L-P model

As illustrated in Fig. 1, the initiation of Loops A and B is facilitated by O_2 dissociation at the dangling bonds of the dimer. In the absence of trapping minority carrier, the dissociation of *paul*-3n occurs spontaneously, resulting in the emergence of $2(P_{b0} + P_{b1})^-$ in the intermediate state of Loop B. Conversely, *paul*-3n leads to SiO_2 growth, thereby enabling the progression of Loop A. The branching between Loops A and B is governed by γ_A. As demonstrated in reference 4, the variable $2(P_{b0} + P_{b1})$ is associated with linear-parabolic growth (Loop L-P). In the Loops A/B & L-P model, X_O is represented analytically as follows, where A_A and A_B, and k_A and k_B, represent the saturation level and reaction coefficient in Loops A and B, respectively. It is noteworthy that A and B in Loop L-P are equivalent to those in Ref. [4].

$$X_O = A_A(1 - e^{-k_A t}) + A_B(1 - e^{-k_B t}) + \frac{1}{2}\left[-A + \sqrt{A^2 + 4B(t - \tau)}\right] \qquad (1)$$

Since Loop L-P has an offset as shown in Fig. 2, the initial values of dX_O/dt upon O_2 introduction are given by $A_A \cdot k_A$ and $A_B \cdot k_B$ for Loops A and B, respectively. They have the following relation with γ_A and O_2 adsorption coefficients of k_{OX} in Loop A and k_{OX1} and k_{OX2} in Loop B [1].

$$R = \frac{k_A \cdot A_A}{k_B \cdot A_B} = \frac{k_{OX}}{k_{OX1} \cdot k_{OX2}} \cdot \frac{\gamma_A}{(1 - \gamma_A)} \qquad (2)$$

R is obtained by fitting X_O with eq. (1) and k_{OX} is the same as k_{XO1} because of O_2 adsorption at V^- for both the cases. As a result, the cooperation mechanism between Loops A and B is considered with γ_A estimated with eq. (3).

$$\gamma_A = \frac{R \cdot k_{OX2}}{1 + R \cdot k_{OX2}} \qquad (3)$$

3. Results and Discussion

As illustrated in Fig. 2, the offset of Loop L-P ranges from 4300 to 5100 seconds, and the slope B/A is negligible. It is evident that Loops A and B demonstrate a substantial discrepancy between p- and n-Si(001) surfaces, as well as between RT and 200°C. It has been observed that Loop A increases rapidly and reaches a state of saturation within the range of 1000 to 2000 seconds. Conversely, Loop B demonstrates a more gradual

increase in its response. These observations imply that the relationship between Loops A and B is contingent on the conduction type and the ambient temperature. The calculation of γ_A is performed using equation (3), as illustrated in Fig. 3, based on the fitting parameters. At RT, γ_A demonstrates a substantial discrepancy: The values 0.252 and 0.339 were obtained for p- and n-Si(001), respectively. When the temperature is increased to 200°C, γ_A decreases down to approximately 0.2 for both surfaces and then increases gradually with temperature. The observed dependence indicates that γ_A is governed by two distinct factors.

The majority carrier trapping process ($V^0 + e^- \rightarrow V^-$) for n-Si(001) yields a dangling bond, which subsequently undergoes hybridization with O_2^-(phys) (• O-O:), thereby forming V^--O_2^{2-}(chem), as depicted in Fig. 4. The formation of *paul*-3n requires the trapping of minority carrier h^+ at V^- for SiO_2 growth, while maintaining electrical neutrality. This is the primary factor of γ_A. The trapping of holes (h^+) is promoted via the Coulomb interaction by O_2^{2-}(chem). The minority carrier trapping of electrons (e^-) at V^+ for p-Si(001) is disturbed by O_2^{2-}(chem). This phenomenon elucidates the observed disparity in the values of γ_A (p-Si) and γ_A (n-Si) at room temperature (RT). It is noteworthy that dissociation of O_2^{2-}(chem) is achieved by hot hole trapping at the bonding orbital σ_g with E_B = 5.1 eV. Electron tunneling from Si CB to O_2(phys) results in the formation of O_2^-(phys) with a single bond, accompanied by the production of hot holes with a maximum energy of ~7 eV through the Auger transition. The occurrence of electron tunneling from O_2^-(phys) to Si is attributed to the energetic instability of O_2^-(phys). The repetition of O_2(phys)⇄O_2^-(phys) during hopping on the surface supplies a number of hot holes, which are responsible for the dissociation of O_2^{2-}(chem). This is the second factor of γ_A. Given the prevalence of hot hole trapping in both p- and n-Si(001), it is anticipated that γ_A (p-Si) and γ_A (n-Si) will exhibit a high degree of similarity, as evidenced by the observations made at temperatures exceeding 200°C in Fig. 3. As the temperature rises, the transition of oxygen molecules between O_2(phys) and O_2^-(phys), known as "hopping," becomes increasingly prevalent. This phenomenon leads to the distribution of hot holes, which are excess energy states in the material, extending beyond the vicinity of V^--O_2^{2-}(chem) and V^+-O_2^{2-}(chem). Conversely, the vibration and rotation of O_2^-(chem) around V^- become effective in collecting hot holes due to the Coulomb force. Consequently, both γ_A (p-Si) and γ_A (n-Si) exhibit an increase in their values with increasing temperatures above 200°C.

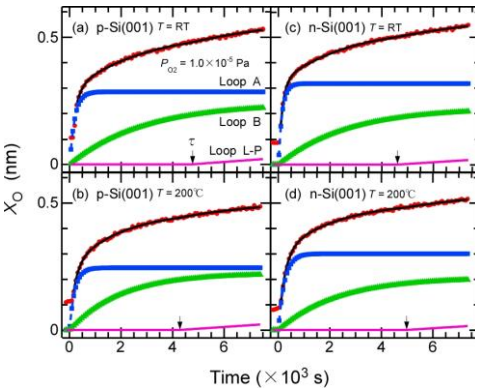

Fig. 2 Curve-fitting analysis of X_O with eq. (1): (a), (b) p-Si(001), and (c), (d) n-Si(001). Arrows indicate the offset of Loop L-P.

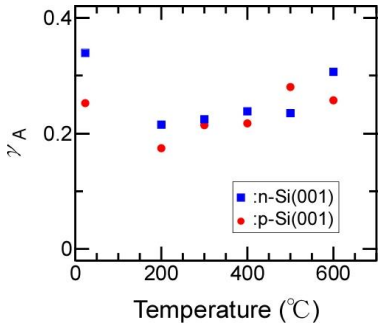

Fig. 3 Temperature dependence of γ_A. k_{OX2} is assumed to be 0.02.

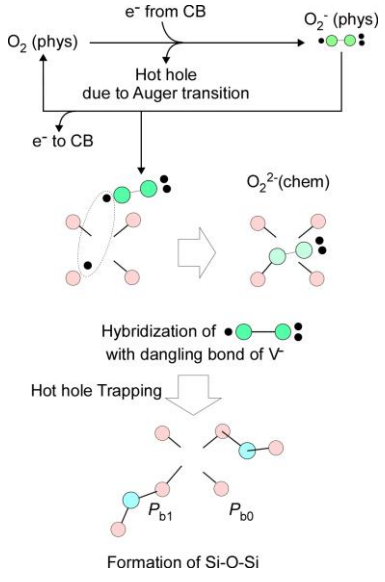

Fig. 4 Trapping-mediated adsorption model of O_2 at V^-.

4. Conclusions

The cooperative process between Loops A and B is facilitated by γ_A, which is governed by minority carrier and hot hole trapping at V^--O_2^{2-}(chem) and V^+-O_2^{2-}(chem). The minority carrier trapping at V^- and V^+ for charge neutrality is the rate-limited step because of insufficient thermal excitation at RT. The distribution of hot holes with temperatures above 200°C is characterized by its extensive nature. Consequently, the process of hot hole trapping at O_2^{2-}(chem) for dissociation becomes predominant in γ_A.

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Segregation induced formation of two-dimensional like GeSn ultra-thin crystal

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1. Introduction

Germanium-based two-dimensional materials such as germanene, and germanium nanosheet (Ge-NS) have attracted attention as channel materials for ultimately miniaturised nanosheet transistors because it has a higher electron mobility and a wider band gap rather than graphene [1,2]. Recently, we have focused on GeSn-NS because Sn incorporation into Ge-NS will achieve a higher electron mobility and a higher band gap than Ge-NS [1,3]. However, GeSn-NS fabrication has not been mostly addressed and achieved yet.

To realize the GeSn-NS formation, we go back to Ge-NS fabrication methods reported so far. Previously, three methods have been mainly addressed: (1) the epitaxial growth on metal surface [4,5], (2) vacuum annealing to germanane chemically synthesised from $CaGe_2$ [6–8], and (3) the segregation from metal/Ge(111) structure e.g., Ag/Ge(111) and Al/Ge(111) [9,10]. Among them, the segregation method using Al/Ge(111) structure has a great merit that the segregated ultra-thin Ge crystal is atmospherically stable because Al_2O_3 cover layer is simulatneously formed on the segregated Ge [10]. However, whether a segregated ultra-thin Ge crystal has two-dimensional structure or not has been still under discussion.

In this study, we demonstrated the GeSn-NS fabrication by the segregation method using Al/$Ge_{1-x}Sn_x$(111) structure. Furthermore, we performed the detail analysis of the crystalline structure of the segregation layer. As a result, we clarified that a GeSn-NS was successfully formed as a segregation layer covered with an Al-oxide layer, and the GeSn-NS showed two-dimensional like structure not a diamond structure.

2. Experimental Procedure

A 3 inch Ge(111) wafer was used as a substrate. We performed chemical cleaning and thermal annealing at 430 °C for 30 min under ultra-high vacuum condition. Then, a ~30-nm-thick $Ge_{0.88}Sn_{0.12}$ epitaxial layer was grown on Ge(111) substrate at 100 °C by molecular beam epitaxy (MBE), and the sample was taken out from the MBE chamber. Next, surface native oxide of the $Ge_{0.88}Sn_{0.12}$ epitaxial layer was removed by HF and HCl mixed solution. Subsequently, thermal cleaning was performed at 300 °C for 30 min under high vacuum condition and a 30-nm-thick Al layer was grown at 100 °C by the vacuum evaporation method in the same chamber. Finally, we performed the post deposition annealing (PDA) at 300 °C for 30 min in an N_2 atmosphere to induce the segreagtion.

3. Results and Discussion

At first, we checked the epitaxial growth of $Ge_{0.88}Sn_{0.12}$ and Al layers by X-ray diffraction, and the segregation of Ge and Sn atoms on the Al layer by X-ray photoelectron spectroscopy (*the results are not shown here*). So next, the crystalline structure of the segeregation layer was analyzed in details using hard-angle annular dark field (HAADF)- and bright-field (BF)-scanning transmission electron microscopy (STEM) observation in conjunction with energy dispsersive X-ray spectroscopy (EDX).

Figures 1(a) and 1(b) showed HAADF-STEM image and point-scan EDX results at four points #1–#4, respectively. From Fig. 1(a), we confirmed that some layered structure was formed. From the point-scan EDX results at #1–#4, each layer from the bottom to the upperside is clarified to correspond $Ge_{0.88}Sn_{0.12}$ epitaxial layer, Al epitaxial layer, the segregation layer, and the Al_2O_3 layer. Particularly, in the segregation layer, both Ge and Sn signals exhibited, meaning the GeSn segregation layer might be formed. The Sn composition of the GeSn segregation layer was estimated to 4.3–7.4%. Although, Al and O signals were also detected in the segregation layer, these signals could be originated from the Al_2O_3 and Al layers because the segregation layer are ultimately thin comparing with the point-scan area.

Next, we discussed the detail crystalline structure of the segregation layer by higher resolution STEM observation. Figures 2(a) and 2(b) show BF-STEM images obtained from the incident direction of $[11\bar{2}]$ and $[1\bar{1}0]$, respectively. We found that the GeSn segregation layer showed two-dimensional like structure with backling shape. However, the lattice spacing of the GeSn segregation layer in the [111] direction is larger than that of the Al layer. This is much more clearly observed in the projected line profiles as shown in Fig. 2(c), which was obtained from the black rectangle area shown in Fig. 2(b). The lattice spacing of the GeSn segregation layer was estimated to 2.6 Å, while that of the Al layer was 2.4 Å. Here, from other STEM results

(*not shown here*), the lattice spacing of the $Ge_{0.88}Sn_{0.12}$ epitaxial layer was estimated to 3.4 Å. Furthermore, the reported values of lattice spacing of germanene and Ge-NS formed on metal layer were ranged from 2.1–2.7 Å [11–16], infering the lattice spacing value of the GeSn segregation layer is well consistent with germanene and Ge-NS. This strongly suggests that the GeSn segregation layer has two-dimensional like structure rather than diamond structure.

4. Conclusions

In this study, we addressed the GeSn-NS formation by the segregation method from the stacked structure of Al/$Ge_{1-x}Sn_x$(111) epitaxial layer. We demonstrated that the GeSn-segregation layer with Sn composition of 4.3–7.4% was formed on the Al layer and that was covered with the Al_2O_3 layer. Furthermore, we firstly showed an evidence of the GeSn segregation layer showed two-dimensional like structure with a lattice spacing of 2.6 Å rather than diamond structure. We believe that this study opens a new door of the segregation method to develop various new materials of group-IV compound NS.

Acknowledgements

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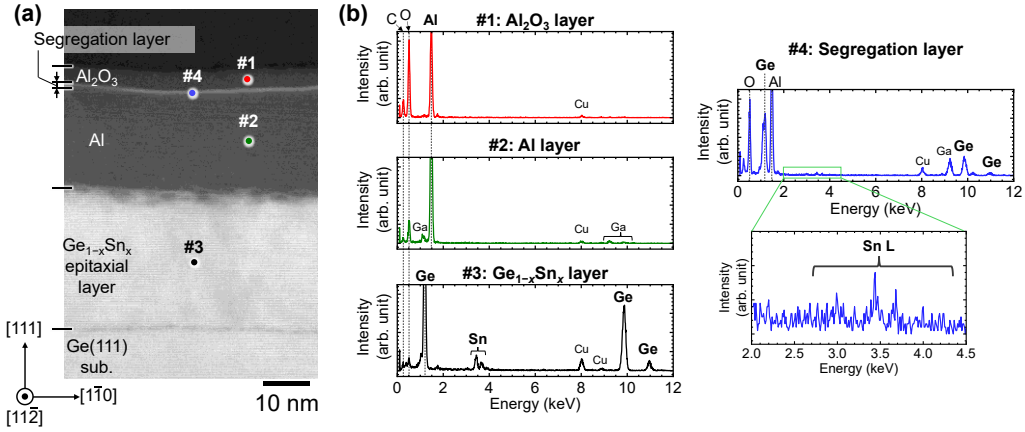

Fig. 1 (a) HAADF-STEM image of the segregated sample. We confirmed that the segregation layer was formed on the Al layer and covered with Al_2O_3 layer. EDX point scan was carried out at #1–#4, and the EDX point scan result of each position is shown in (b). We verified that both Ge and Sn exhibited in the segregation layer.

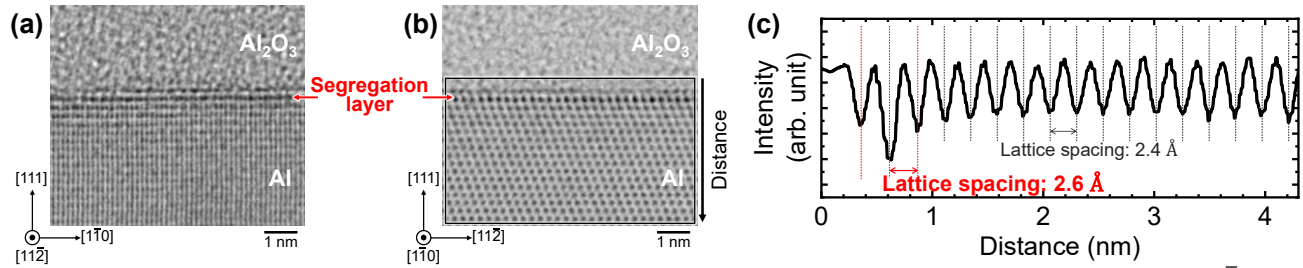

Fig. 2 High resolution BF-STEM images of the segregated sample obtained with the incident direction of (a) [11$\bar{2}$] and (b) [1$\bar{1}$0]. The projected line profile was obtained from the black rectangle area in Fig. 2(b) with the direction from Al_2O_3 to Al, which is shown by the black arrow. The obtained profile was shown in (c). We found that the lattice spacing of the segregation layer is clearly different with the Al layer.

Role of Annealing Atmosphere Towards Stoichiometry and Chemical Integrity of Solution-Processed MoS_2 Thin Films

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1. Introduction

Among various approaches, solution process is one of the quickest and simplest methods to produce MoS_2 thin films, compared to other techniques such as chemical vapor deposition (CVD), atomic layer deposition (ALD), and mechanical exfoliation [1-3]. However, their stoichiometry and chemical integrity are typically affected by sulfur vacancies (V_s) that serve as reactive sites for oxygen incorporation and cause degradation in device performance [4]. Annealing in sulfur vapor (S-vapor) represents a promising technique toward the restoration of stoichiometry through sulfur replenishing and concurrent oxidation suppression. Herein, we demonstrate the solution-based synthesis of MoS_2 films on Si_3N_4 surfaces with various precursor concentrations (5, 12, 16, 20, 25, and 30 mM) followed by annealing in argon (Ar) and sulfur vapor (S-vapor) at 700 °C. S-vapor annealed films achieved a near-ideal S/Mo ratio (~2:1) with significantly lower oxidation than Ar-annealed films, indicating the strong influence of annealing atmosphere on the stability of MoS_2 .

2. Experimental Procedure

Molybdenum disulfide (MoS_2) films were prepared from a precursor solution via a single-step annealing in Ar and S-vapor atmospheres. The precursor solution was obtained by dissolving ammonium tetrathiomolybdate [$(NH_4)_2MoS_4$, 99.999%, Sigma Aldrich] in a solvent mixture of dimethylformamide (DMF), isopropanol (IPA), and ethanolamine with the 3:5:3 (v/v) ratio. The solution was stirred for 2 h, and spin-coated on clean Si_3N_4 surfaces at 500 rpm for 10 s and 3000 rpm for 30 s. The Si_3N_4 surfaces were treated with 0.5% HF for 60s followed by rinse with DI water. The films were pre-annealed at 180 °C for 30 min and annealed at 700 °C for 1 h under 1 slm Ar flow using a lamp annealing system. S-vapor annealing procedures are demonstrated in Fig.1. The fabricated MoS_2 films were characterized using transmission electron microscopy (TEM), Raman spectroscopy, x-ray photoelectron spectroscopy (XPS) and thermal desorption spectroscopy (TDS) respectively.

3. Results and Discussion

To assess the stoichiometry and sulfur vacancy (V_s) of the MoS_2 films, X-ray photoelectron spectroscopy (XPS) measurements were performed on both the surface and after 15 s etching, as illustrated in Fig. 2. At 5 mM, both films show sulfur deficiency (S/Mo ~2:1), but Ar-annealed films (Fig. 2a) remain sub-stoichiometric across all concentrations. In contrast, S-vapor annealed films (Fig. 2b) approach the ideal 2:1 ratio with increasing concentration and achieve homogeneous stoichiometry above 12 mM. These results confirm the effectiveness of S-vapor annealing in mitigating sulfur vacancies [5], despite minor surface oxidation upon air exposure.

The Mo^{6+}/Mo^{4+} ratios of Ar and S-vapor annealed MoS_2 films were obtained from the Mo 3d XPS spectra (Fig. 3). Ar-annealed MoS_2 films (Fig. 3a) undergo significant oxidation, with Mo^{6+}/Mo^{4+} ratios reaching a maximum at ~0.45 around 16 mM and persisting even after etching, indicating interfacial defects and oxygen incorporation. In contrast, S-vapor annealing keeps the ratio below 0.2 (slightly higher at the surface), yielding stoichiometric and chemically stable films above 12 mM as illustrated in Fig. 3b. These results confirm the superior oxidation resistance of S-vapor annealed MoS_2. Sulfur vacancies in MoS_2 strongly affect its electronic properties and also promote environmental degradation through oxidation. To investigate the impact of these vacancies and the subsequent adsorption of O_2 and H_2O molecules, density functional theory (DFT) calculations were performed as shown in Fig. 4. PDOS analysis shows that pristine MoS_2 with a band gap (E_g) of 1.7 eV, has a S-3p dominated valence band and a Mo-4d dominated conduction band with no mid-gap states. Introducing a sulfur vacancy reduces the band gap to 1.3 eV and creates Mo 4d defect states near the Fermi level. O_2 adsorption slightly recovers the gap (1.5 eV) but leaves residual states, indicating poor passivation. In contrast, H_2O adsorption restores the gap to 1.74 eV, effectively suppressing defect states and providing better passivation.

4. Conclusions

In conclusion, S-vapor annealing is essential for repairing sulfur vacancies, suppressing oxidation, and achieving near-stoichiometric, crystalline MoS_2 films. This post-synthesis treatment offers a reliable route to structurally and chemically stable MoS_2 for future electronic applications.

Acknowledgements

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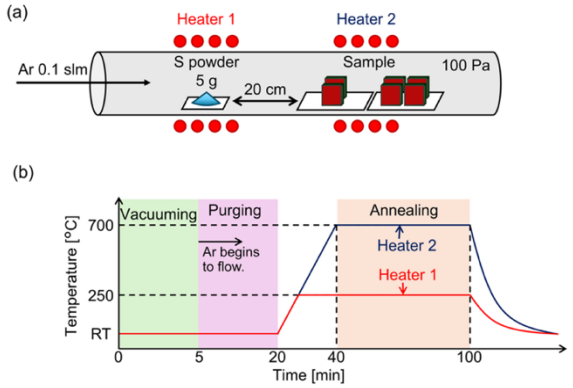

Fig. 1: (a) Schematic of the two-zone furnace setup used for sulfur annealing of MoS_2 films and (b) Temperature vs time profile of annealing process.

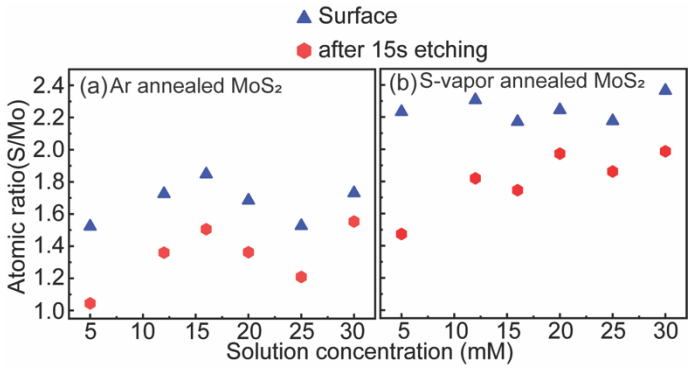

Fig. 2: Sulfur-to-molybdenum (S/Mo) atomic ratio of MoS_2 films as a function of precursor concentration, extracted from XPS of Mo 3d: (a) Ar-annealed and (b) S vapor-annealed films at 700 °C.

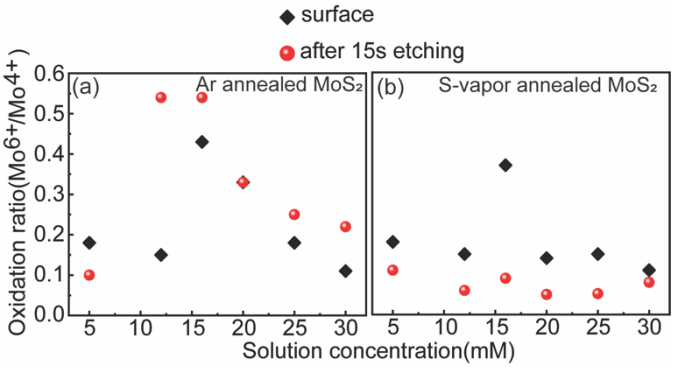

Fig. 3: Mo^{6+}/Mo^{4+} ratio as a function of solution concentration, extracted from Mo 3d XPS spectra of MoS_2 films grown on Si_3N_4 surfaces using (a) Ar annealing and (b) S vapor annealing at 700 °C.

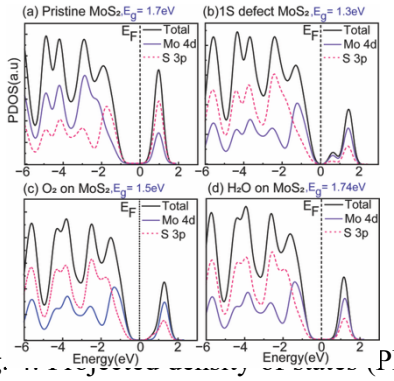

Fig. 4: Projected density of states (PDOS) (a) Pristine MoS_2 (b) Sulfur defect (1S) defect MoS_2 (c) O_2 adsorbed MoS_2 and H_2O adsorbed MoS_2 respectively.

Focus Session | Electrically / Physicaly Characterization

Fri. Nov 7, 2025 10:55 AM - 11:55 AM JST | Fri. Nov 7, 2025 1:55 AM - 2:55 AM UTC 5F-Meeting Room

[FB] Focus Session B ~ Device Properties under Cryogenic Temperature

Chair:Akio Ohta(Fukuoka University), Takezo Mawaki(Tohoku University)

10:55 AM - 11:25 AM JST | 1:55 AM - 2:25 AM UTC

[FB-01]

(invite)Demonstration of Recovery Annealing on 7-Bits per Cell 3D Flash Memory at Cryogenic Operation for Bit Cost Scalability and Sustainability

*Yuta Aiba[1] (1. Frontier Technology Research & Development Institute., Kioxia Corporation (Japan))

11:25 AM - 11:55 AM JST | 2:25 AM - 2:55 AM UTC

[FB-02]

Toward Stable Operation of Si Quantum Computers: Origin of Long-period Charge Fluctuations in Si Fin-type Quantum Dots

*Hiroshi Oka[1], Hidehiro Asai[1], Kimihiko Kato[1], Takumi Inaba[1], Shota Iizuka[1], Yusuke Chiashi[1], Hitoshi Yui[1], Shoko Nagano[1], Shigenori Murakami[1], Yoshihisa Iba[1], Minoru Ogura[1], Takashi Nakayama[1], Hanpei Koike[1], Hiroshi Fuketa[1], Satoshi Moriyama[2], Takahiro Mori[1] (1. AIST (Japan), 2. Tokyo Denki Univ. (Japan))

(invite)Demonstration of Recovery Annealing on 7-Bits per Cell 3D Flash Memory at Cryogenic Operation for Bit Cost Scalability and Sustainability

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1. Introduction

NAND Flash memory is one of the lowest cost and highest bit density nonvolatile memory [1, 2]. Although the bit cost scaling has been achieved so far by highly stacked word lines (WL), the increase of fabrication cost will make it difficult in near future. Therefore, there is a need for an alternative scaling technology without increasing the process steps and fabrication cost, such as the multi-level cell [3] (Fig. 1). We previously reported that cryogenic operation of 3D flash memory at 77 K could achieve 6-bits [4], and 7-bits per cell by utilizing epi-Si channel [5]. However, it was based on a relatively fresh device before P/E cycle degradation, and therefore reliability characteristics remains to be improved for practical use. In this report[6], we describe that the P/E cycle degradations of cell characteristics can be recovered by annealing and present a novel countermeasure to achieve reliable 7-bits per cell operation.

2. Experimental Result

We conducted an experiment to evaluate the storage performance degradation caused by write/erase cycles at cryogenic temperature and apply recovery annealing. As a result, we found that a relatively low temperature and short annealing time of 3 hours at 200°C with appropriate data written during annealing can fully recover memory cell characteristics. Fig.2 shows a successful demonstration of 7-bits per cell at 77 K after 2 times of both P/E 10 k cycles and recovery annealing. Even after a total 20k write/erase cycles, a tight distribution of 128 Vths (equivalent to 7 bits) was achieved, with performance equivalent to the initial state. Fig.2 shows the degradation of program noise due to P/E cycles and recovery after annealing. The effect of recovery annealing is repeatable, indicating that the memory chip can be reusable. Fig.3 shows the bit cost, which includes bit fabrication cost and cryogenic cooling cost. Reuse enabled by the recovery annealing can further reduce bit cost since there is no need for fabrication. It becomes one-half or one-third by reusing a device 2 times or 3 times, respectively.

3. Conclusions

In this paper, 7-bits per cell at cryogenic operation of 77 K combined with the recovery annealing is reported. These technologies can make the future 3D flash memory further bit-cost scalable and sustainable.

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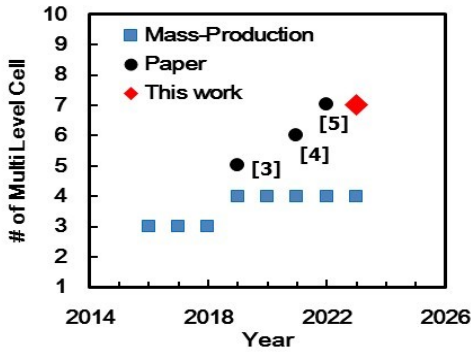

Fig. 1 Multi-level cell has been achieved continuously from 5-bits per cell to 7-bits per cell.
[6] Y. Aiba et al., VLSI, pp.1-2 (2023)

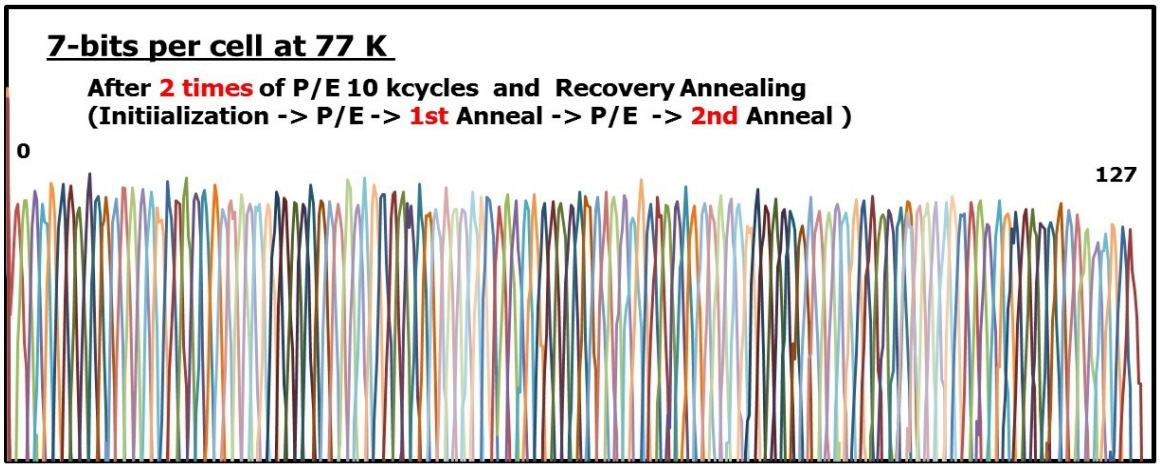

Fig. 2 Demonstration of 7-bits per cell at 77 K with epi-Si channel after 2 times of both P/E 10k cycles and recovery annealing.
[6] Y. Aiba et al., VLSI, pp.1-2 (2023)

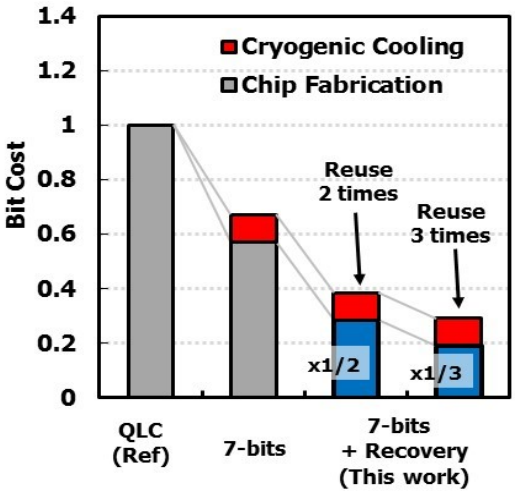

Fig.3 Future bit cost scaling is achieved by both 7-bits per cell at cryogenic operation and reuse by applying recovery annealing.
[6] Y. Aiba et al., VLSI, pp.1-2 (2023)

Toward Stable Operation of Si Quantum Computers: Origin of Long-period Charge Fluctuations in Si Fin-type Quantum Dots

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1. Introduction

Si quantum computers (QCs) have attracted considerable attention due to their scalability potential to achieve the large-scale integration of Si spin qubits using CMOS manufacturing technology. Recently, there has been several progresses in the performance of Si spin qubits, such as two-qubit gates operation with fidelity over 99%[1] and prolonged coherence time T_2^* of 120 μsec [2]. From the standpoint of practical use, the electrical stability of qubits is a critical issue that needs to be addressed, as they necessitate frequent monitoring and calibrations of the qubit parameters (Fig. 1). Indeed, some superconducting QCs already in commercial use are calibrated every few hours, preventing the stable operation and limiting the available time slot. However, the electrical stability of Si spin qubits, i.e., long-period charge fluctuation, has not been thoroughly discussed until now. In this study, we conducted an in-depth analysis of the electrical stability of the fin-type Si quantum dots (QDs), which is a promising host for spin qubits. We performed gate-bias-dependent random telegraph noise (RTN) measurements to clarify the physical origin of the long-period charge fluctuation of fin-type QDs for the first time.

2. Experimental Procedure

Fin-type QDs were fabricated on p-type SOI wafers (T_{SOI}=60 nm, T_{BOX}=145 nm) with a 12-nm-thick SiO_2/poly-Si gate (Fig. 2). A plunger gate (PG), barrier gates (BGs), and accumulation gates (AGs) were formed on the fin to confine electrons under the PG. The measurements were performed at 4 K using a cryogenic prober. We confirmed successful single-electron transport at 4 K with fabricated fin-type QDs from the charge stability diagram shown in Fig. 3(a). Figure 3(b) shows the drain current (I_D) transient at a fixed gate bias. A distinct two-level transition was observed with an ultralow frequency of < 0.05 Hz, which would become a critical issue for the stable operation of Si QCs. As the QDs have multiple gates and different bias conditions are used for single-electron transport, it is very difficult to identify the origin of charge fluctuation by the QD measurement alone. Thus, we fabricated the single-gate test device having the same fin and gate structure as QDs, enabling the gate-bias-dependent RTN analysis to reveal the trap states inducing the long-period charge fluctuations (Fig. 4).

3. Results and Discussion

Figure 5(a) shows the I_D-V_G characteristic of a single-gate test device at 4 K. Captured I_D transients at different gate bias conditions from off-state to on-state bias are shown in Figs. 5(b) to 5(g). A distinct multi-level transition was observed at bias conditions of 300, 320, and 340 mV. These are close to V_{th} of 320 mV, and we confirmed the long-period charge fluctuation occurred only at certain bias conditions. We extracted the power spectral density (S_{ID}) from the Fourier transform of the I_D transient (Fig. 6). The S_{ID} showed drain current dependence and increased by more than one order of magnitude toward V_{th}. As the S_{ID} is proportional to the effective trap density (N_{eff}) in the carrier number fluctuation (CNF) model [3], the obtained results indicate that N_{eff} is increased near V_{th}. From the fitting of the S_{ID} -I_D plot based on the CNF model, we extracted the energetic distribution of trap states inducing excess noise near V_{th}. We found the exponentially distributed trap states with shallow decay energy of 20 meV at the conduction band edge are responsible for the charge fluctuation observed near V_{th} (Fig. 7). To reveal where long-period charge fluctuation occurs in fin-type QDs, we performed a simulation of single-electron transport by using an in-house TCAD simulator [4]. Figure 8 shows the simulated Fermi level (E_F) position along the fin-width (A-B) and fin-depth (A-C) directions. We found the E_F aligns to the band edge states in the whole area of the top-surface of the fin, while that of the side-surface is mostly far from the band edge states. This means the long-period charge fluctuations mainly occur at the top-surface of the fin rather than its side-surface. Since the band edge states are strongly related to the quality of the MOS interface [5], these results imply that the MOS interface engineering at the top-surface of the fin is critical to improve the electrical stability of the fin-type QDs.

4. Conclusions

We conducted the first experimental verification on the long-period charge fluctuation of fin-type QDs, whose origin is band edge states located at the top-surface of the fin, suggesting that even more care of the MOS interface at the fin-top is necessary to provide better stability. We believe that the obtained knowledge paves the way to realize stable quantum computation with Si spin qubits.

Acknowledgements This work is based on the results obtained from the MEXT Q-LEAP Grant No. JPMXS0118069228, Japan.

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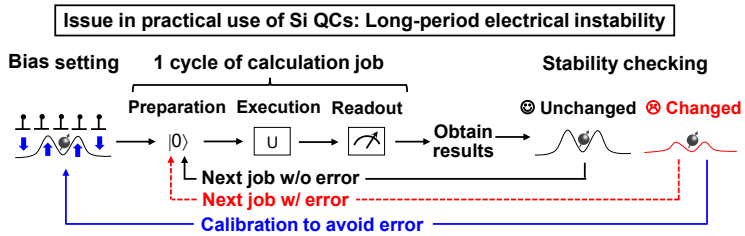

Fig. 1 The aim of this study is to clarify the origin of long-period charge fluctuation of Si QDs that necessitates frequent monitoring and calibration during its running time.

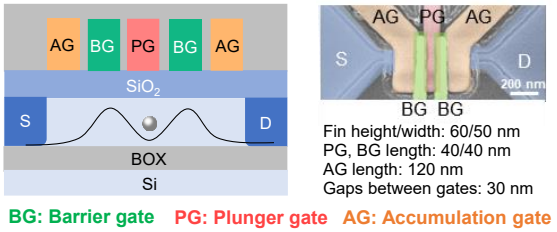

Fig. 2 Fabricated fin-type QDs on SOI wafer. The gate bias condition was chosen to confine an electron using a potential barrier formed by PG, BG, and AG.

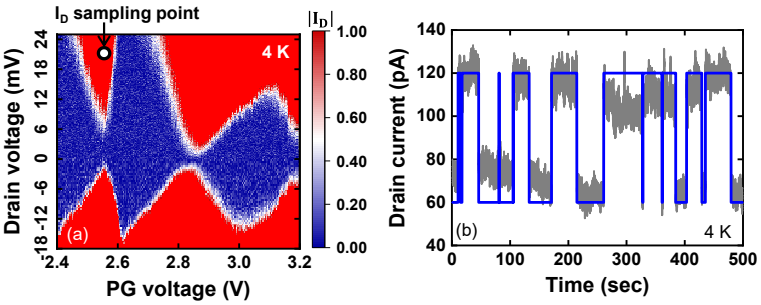

Fig. 3 (a) Charge stability diagram of fin-type QDs. (b) I_D transient of fin-type QDs with gate bias condition indicated in (a).

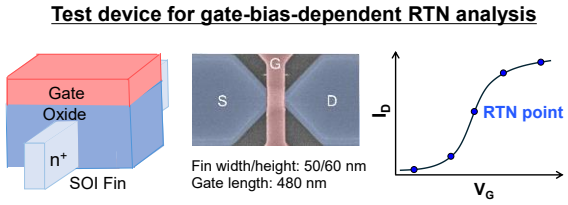

Fig. 4 Single-gate test device, which is fabricated on the same wafer with the same process as the fin-type QDs. Gate-bias-dependent RTN analysis was conducted to clarify the origin of charge fluctuation.

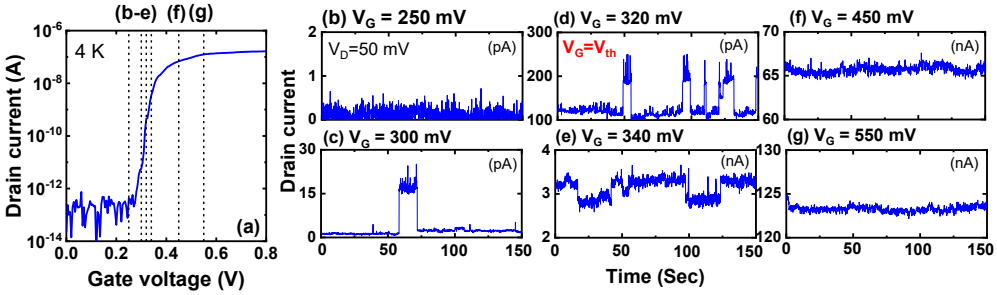

Fig. 5 (a) I_D-V_G curve and transient of I_D of single-gate test device at 4 K with gate bias of (b) 250 mV, (c) 300 mV, (d) 320 mV, (e) 340 mV, (f) 450 mV, and (g) 550 mV. Trapping/de-trapping events observed only near the V_{th} operation.

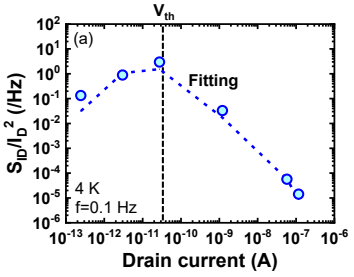

Fig. 6 I_D dependence of S_{ID}/I_D^2. Excess noise appeared near V_{th}. The fitting curve is also shown.

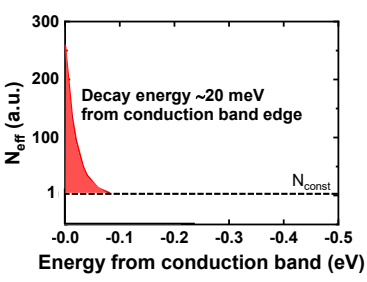

Fig. 7 Extracted energetic distribution of trap states from fitting of S_{ID} shown in Fig. 6.

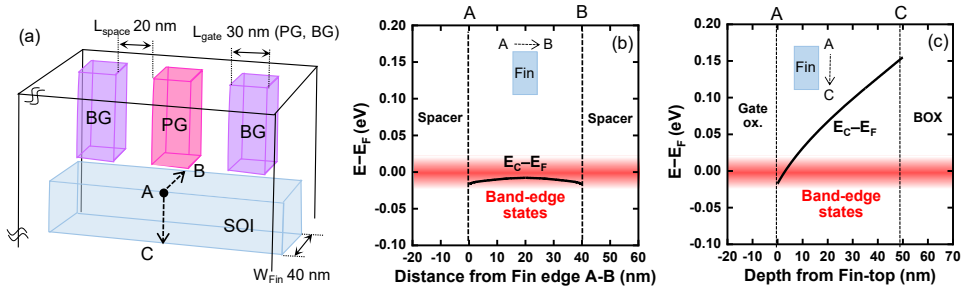

Fig. 8 (a) Structure of simulated fin-type QDs. Simulated energy level of E_C relative to E_F (E_C–E_F) along with (b) fin width A-B and (c) fin depth A-C. Position for conduction band edge operation (E_F–E_C <20 meV) is marked by red areas.

Power Device & Processes | Electron device, process, and characterization

Fri. Nov 7, 2025 1:30 PM - 3:10 PM JST | Fri. Nov 7, 2025 4:30 AM - 6:10 AM UTC 5F-Meeting Room

[S6] Power Device & Processes (1)

Chair:Motoyuki Sato(Tokyo Electron), Toshinori Numata(Toyota Technological Institute)

1:30 PM - 2:00 PM JST | 4:30 AM - 5:00 AM UTC

[S6-01]

Carbon P_b centers in 4H-SiC/SiO_2 interface

*Takahide Umeda Umeda[1], Mitsuru Sometani[2], Bunta Shimabukuro[1], Yusuke Nishiya[3], Yu-ichiro Matsushita[3] (1. Univ. of Tsukuba (Japan), 2. AIST (Japan), 3. Quemix Inc./Tokyo Univ. (Japan))

2:00 PM - 2:20 PM JST | 5:00 AM - 5:20 AM UTC

[S6-02]

Study on Possible Origin of Improved 4H-SiC (0001) MOS Interface Characteristics with Direct NO Oxynitridation Based on Consideration of Oxinitride Growth Kinetics

*Yutaro Uchida[1], Atsushi Tamura[1], Koji Kita[1] (1. The Univ. of Tokyo (Japan))

2:20 PM - 2:40 PM JST | 5:20 AM - 5:40 AM UTC

[S6-03]

Impact of Substrate-Surface Oxidation Treatment and Post-Deposition Annealing on β-Ga_2O_3 (001) MOS Interfaces with ALD-Deposited Al_2O_3 and SiO_2

*Atsushi Tamura[1], Hayama Imaida[1], Hiroyasu Maekawa[2], Koji Kita[1,2] (1. Dept. of Advanced Materials Science, The Univ. of Tokyo (Japan), 2. Dept. of Materials Engineering, The Univ. of Tokyo (Japan))

2:40 PM - 3:10 PM JST | 5:40 AM - 6:10 AM UTC

[S6-04]

Exploration of new materials for meta-materials and power semiconductor applications

*Kentaro Kaneko[1] (1. Ritsumeikan Univ. (Japan))

Carbon P_b centers in 4H-SiC/SiO_2 interface

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1. Introduction

Out invited talk focuses on new and published results for carbon P_b centers ("the P_{bC} centers") in SiC MOS (metal-oxide-semiconductor) structures. The P_{bC} center is a carbon version of the famous P_b centers (Si dangling bonds) at Si/SiO_2 interfaces [1], and we can point out not only many similarities between P_{bC} and P_b but also their dissimilarities, in other words, differences between SiC and Si.

Before presenting the P_{bC} centers, we would like to introduce 4H-SiC material itself. 4H-SiC is a wide-gap semiconductor (E_g = 3.26 eV), showing many unique and interesting properties; such as its useful MOS structure with thermal oxidation, a wide-range capability of ion-implantation doping from *n*+ to *p*+, large-sized single-crystal wafers, etc. These features make 4H-SiC being a leading wide-gap semiconductor for the next-generation power electronics, enabling its industrial applications to inter-city transportations (e.g., Yamanote-Line), high-speed trains (e.g., Shinkan-sen N700S), and electric vehicles (e.g., Tesla EVs), and so on. The power 4H-SiC MOSFETs with 600V or 1200V voltage range are representative devices. Such power MOSFETs, however, still suffer from many unresolved issues in their performance and reliability. Most of the issues are related to MOS interface defects or interface states (Dit). Therefore, many studies continuously challenge to clarify origins of Dit, how to control (remove) them, and their roles/influences on SiC MOSFETs. The P_{bC} center shown here is a unique example in wide-gap semiconductors, whose properties (origin [2], density [3], energy levels [4], reactivity [3,5,6], etc.) are clearly revealed as comparable as those of the P_b center in Si-MOS systems.

2. What is the P_{bC} center?

The P_{bC} center was found in 4H-SiC(0001) face ["Si face", Fig. 1(a)] after thermal oxidation. We can observe it by using electron-spin-resonance (ESR) or electrically-detected ESR (EDMR) spectroscopy. Its origin is a carbon dangling bond normal to the Si face [2] [Fig. 1(b)], which looks like very similar to the famous P_b center at Si(111)/SiO_2 interfaces [1] [Fig. 1(c)]. They are assigned to be $Si_3{\equiv}C\bullet$ and $Si_3{\equiv}Si\bullet$, respectively ("•" indicates an unpaired spin). Their typical densities are comparable: $3{-}4{\times}10^{12}$ cm^{-2} [3] and $1{-}4{\times}10^{12}$ cm^{-2} [1], despite 4H-SiC(0001) lattice is much denser than that of Si(111). This comparability suggests more efficient structural relaxation around P_{bC} as compared to the case of P_b. We pointed out that the P_{bC} center is formed at a carbon adatom (C_{adatom}) on the Si face. This structure has a great advantage of decreasing Si bonds to the SiO_2 layer [Fig. 1(b)], leaving a single dangling bond on C_{adatom}. Furthermore, it has another merit to utilize residual carbon atoms emitted during the oxidation process. Figure 1(d) shows an enlarged view (×10) of an EDMR signal of the P_{bC} center. We successfully detected hyperfine (HF) splittings due to ^{13}C nuclear spin at C_{adatom} and ^{29}Si nuclear spins at three Si back-bonds. The observed HF splittings well agreed with the theoretical ones for the C_{adatom} structure [2]. Furthermore, we also revealed chemical reactivities of P_{bC} for many processes, like shown in Fig. 1(e) [3,5,6].

Energy levels of P_{bC} have been experimentally determined [4], likewise the case of P_b. The P_{bC} center shows three possible charge states, +1 (no electron/spin=0), 0 (one electron/spin=1/2), and -1 (two paired electrons/spin=0), as shown in Fig, 1(f). Thus, the (+/0) and (0/-) levels are determined to be E_V+0.6 eV and E_V+1.2 eV, respectively. This is the world-first data on a direct relationship between Dit and interface defects in wide-gap semiconductors. Using this benchmark result, we also examine highly-accurate first-principles calculations (based on HSE06 functionals) on P_{bC} [4]. The calculated results are also shown in Fig. 1(f), where we find a significant discrepancy, indicating a limitation that the state-of-the-art calculations still include problems for predicting interface states.

3. Two types of the P_{bC} centers

On 4H-SiC(0001) face, there is another P_{bC} center, which we name "P_{bC}-type2 center." As shown in Fig, 1(f), the primary type noted above (we call it "P_{bC}-type1" hereafter) has E_V-side interface states. On the other hand, the P_{bC}-type2 center exhibits E_C-side interface states [7]. The reasons why two types of P_{bC} exist in 4H-

SiC, why their energy levels are so different, and what are their influences on 4H-SiC MOSFETs, are discussed in the presentation.

Acknowledgements

This work was supported by CSTI SIP program, "Next-generation power electronics", and also partly by MEXT Grant-in-Aids 18H03770, 18H03873, 17H02781, 20H00340, 21H04553 and JP-MXP1020200205. The authors also acknowledge many other collaborators listed as co-authors in our published papers.

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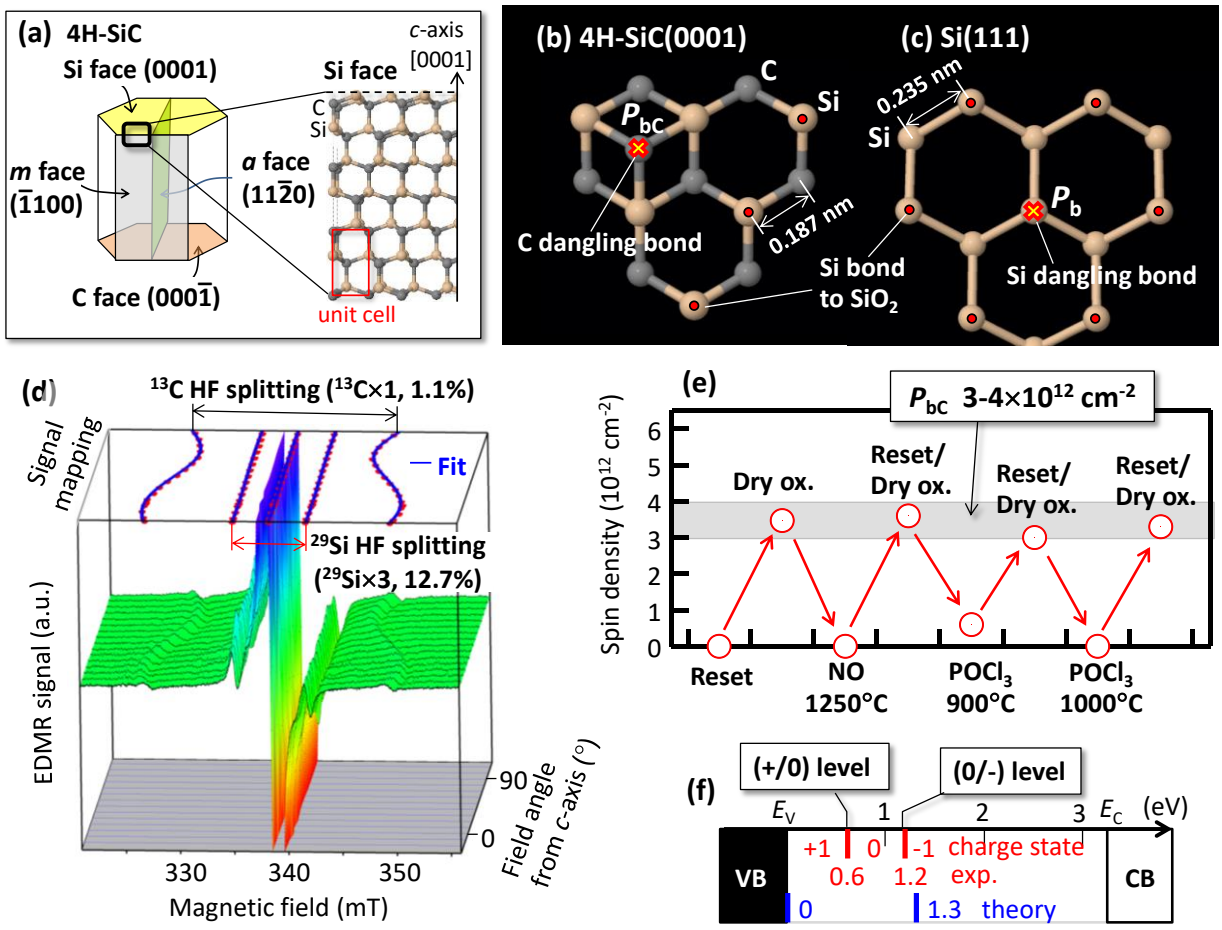

Fig. 1 The carbon P_b center (P_{bC} center) at 4H-SiC(0001)/SiO_2 interface. (a) 4H-SiC single-crystal system. (b) P_{bC} center at 4H-SiC(0001) face. (c) P_b center at Si(111) face. (d) EDMR spectra of P_{bC} observed using dry-oxidized 4H-SiC(0001) MOSFET (maximum field-effect mobility = 8 $cm^2/V/s$) [2]. (e) Chemical reactivity of P_{bC} [3]. (f) Energy levels of P_{bC} [4].

Study on Possible Origin of Improved 4H-SiC (0001) MOS Interface Characteristics with Direct NO Oxynitridation Based on Consideration of Oxinitride Growth Kinetics

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1. Introduction

In SiC power MOSFETs, one of the commonly employed methods to form MOS interfaces is the thermal oxidation, followed by NO annealing which enables an efficient passivation of MOS interface defects by replacing a part of the topmost C atoms on SiC by N. The N density introduced by this process is known to be saturated to a certain value [1]. On the other hand, the direct NO oxynitridation of 4H-SiC substrates to form a SiO(N) film has a potential to be an alternative process [2]. Since the kinetics of the N atom introduction on SiC surface should differ between the direct nitridation on the surface and the nitridation through a thick-SiO_2 layer, the electrical properties of the formed interfaces will be also different. In this study, we investigated both the kinetics of the direct NO oxynitridation and the interface characteristics of MOS capacitors employing the oxynitride as the interface layer.

2. Experimental Procedure

4° off-axis n-type 4H-SiC (0001) Si-face wafers with epitaxial layers (N_D ~1×10^{16} cm^{-3}) were used as substrates. After cleaning in diluted HF, the wafers were directly oxynitrided at 1150°C for various durations in NO:N_2=1:2 ambient to form SiO(N) films. The grown film thickness and N density on SiC substrate were evaluated by X-ray reflectivity and a ratio of N 1s / Si 2p XPS intensities, respectively. Next, on the SiO(N) film formed by direct NO oxynitridation as described above, a 15-nm-thick-Al_2O_3 layer was deposited at 250°C with atomic layer deposition using TMA and H_2O as oxidant as shown in **Fig. 1**. Subsequently, the samples were annealed in 0.1%-O_2+N_2 ambient at 400－600°C, followed by a deposition of Au electrodes to form MOS capacitors. For comparison, a sample was also fabricated by thermal oxidation in O_2 followed by NO annealing at 1150°C for 120 min.

3. Results and Discussion

The time dependent change of SiO(N) film thickness grown on the substrate by the direct NO oxynitridation is shown in **Fig. 2(a)**. In the initial 10 min, the growth rate of the SiO(N) film by direct NO oxynitridation at 1150°C was high, to achieve a film thickness of ~2.5 nm rapidly. After that it slowed down significantly and the film thickness reached only about 5 nm even after as long as 120 min oxynitridation. Next, the SiO(N) films were removed by HF etching, and the N density on SiC substrate surface was evaluated by XPS. The density shown on the righthand side axis in **Fig. 2(a)** was estimated based on the previously determined relationship between N 1s / Si 2p intensity ratio and the surface N areal density determined by high-resolution RBS in our group. The nitrogen incorporation proceeds rapidly in the initial stage, with the surface N areal density reaching ~1.7×10^{14} cm^{-2} within 10 minutes, after which it quickly saturates. It is different from a gradual increase of N density for the case of conventional NO annealing of a thick-SiO_2/SiC stacks [1] (data not shown). It should be noted that the ratio of the oxidation rate to the nitridation rate is small in the initial stage with rapid nitrogen incorporation but significantly increases in the latter stage as will be discussed later. The N 1s core level XPS after removal of surface oxide is shown in **Fig. 2(b)** for the oxynitridation durations of 10 min (NO10) and 120 min (NO120). Compared with NO10, the peak of NO120 shifts to a lower binding energy by ~0.2 eV when the binding energy was calibrated by the Si 2p substrate peak. It is considered that N−Si bonds are predominant in NO10, whereas the fractrion of N−O bonds increases in NO120.

The energy distributions of D_{it} determined by the conductance method for the MOS capacitors after PDA at 400°C are shown in **Fig. 3(a)**. It should be noted that NO120 showed a lower D_{it} than the reference sample of conventional NO annealing after thermal oxidation (Thermal+NO), while the NO10 exhibited a higher D_{it} than that. This indicates that the long-time oxynitridation is required to reduce the interface trap density, although the relatively high N surface density was achieved even with a short-time direct NO oxynitridation. **Fig. 3(b)** shows the comparison of D_{it} at $E = E_c - 0.2$ eV for Al_2O_3/SiO(N)/4H-SiC(0001) MOS capacitors annealed in 0.1%-O_2+N_2 ambient at 400°C or 600°C. This result revealed that PDA at 600°C leads to a slight increase of D_{it} from that obtained at 400°C, while D_{it} value remains comparable to that of Thermal+NO, which indicates that the passivation process of SiO_2/SiC interface defects by NO does not have to be conducted as the final step of the process.

Figure 4(a) shows the relationship between the N surface density on SiC and D_{it} at $E = E_c - 0.2$ eV. The dashed line in the figure represents the trend of the results obtained by our previous work for the cases of annealing of thermal oxide films in N_2+O_2 ambient under various conditions [3]. It revealed that D_{it} of NO120 was approximately one third of the value expected from the trend of the previous work for the identical surface N density, indicating that the improved interface characteristics of the NO120 should not be attributed solely to the increase in surface N density.

The origins of the improved interface quality with a lower D_{it} of NO120 would be explainable by two possible factors. First, the growth rate of the SiO(N) film significantly slows down at ~2.5 nm as discussed above, and the oxidation of SiC proceeds slowly in the latter stage of the oxynitridation. Since such a SiO(N) layer would be thin enough for the carbon byproduct desorption through the layer, more efficient desorption of excess C atoms at the interface would occur, enabling a further reduction of the interface defect density (**Fig. 4(b)**). Second, as shown in **Fig. 4(c)**, the ratio of the oxidation rate to the nitridation rate significantly increases in the latter stage. The formation of interface with not only N−Si but also a certain fraction of N−O bonds may play a role in stabilizing the N-passivated interface structure and enhancing the interface properties.

4. Conclusions

The direct NO oxynitridation of SiC surface forms a nanometer-order SiO(N) interlayer for advanced SiC MOS stacks. Sufficiently long duration of the direct NO oxynitridation resulted in the formation of the interface with lower D_{it} than the conventional NO annealing method when compared for the same interface N density. In contrast, the short-time direct oxynitridation does not improve interface properties, possibly because the prolonged oxynitridation is required to modify the interface structure where the N-passivation works more efficiently.

Acknowledgements

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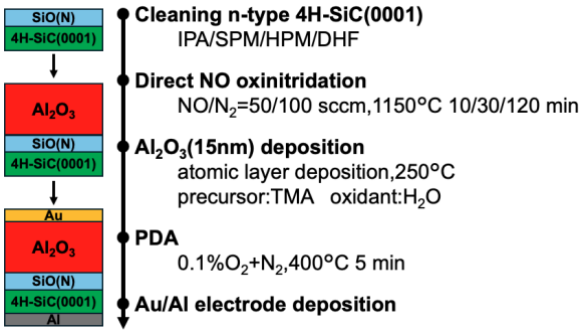

Fig. 1 The fabrication process of Al_2O_3/SiO(N)/4H-SiC(0001) MOS capacitors.

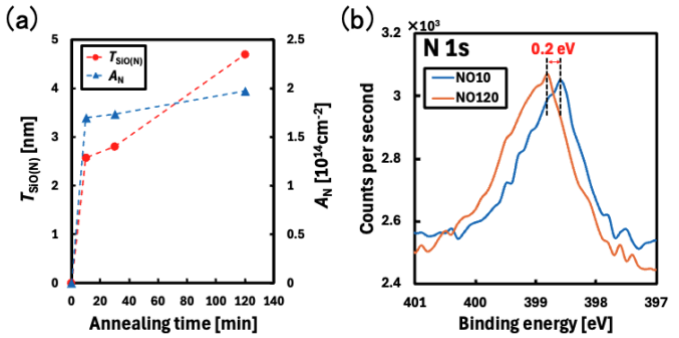

Fig. 2 (a)Relationship between direct NO oxynitridation time and SiO(N) film thickness($T_{SiO(N)}$) (red circles), and N density at SiC surface(A_N) (blue triangles). (b) N 1s XPS core level spectra of NO10 and NO120 after removal of SiO(N) layer by HF.

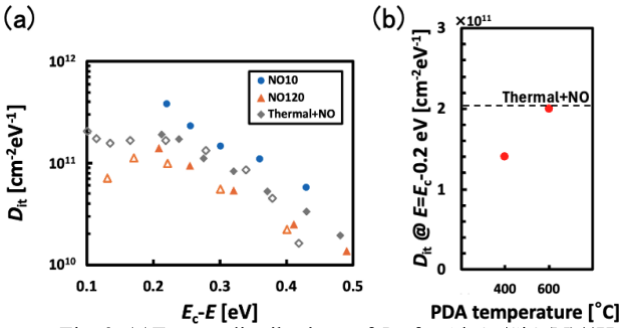

Fig. 3 (a)Energy distributions of D_{it} for Al_2O_3/SiO(N)/4H-SiC(0001) (NO10 and NO120) and SiO_2/4H-SiC (0001) (Thermal+NO) MOS capacitors. Outline symbols show the results measured at −50°C while others were determined at RT. (b)Comparison of D_{it} at $E = E_c - 0.2$ eV for Al_2O_3/SiO(N)/4H-SiC(0001) MOS capacitors annealed in 0.1%-O_2+N_2 ambient at 400°C or 600°C.

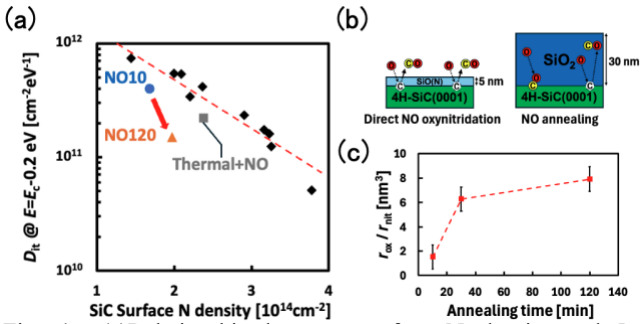

Fig. 4 (a)Relationship between surface N density and D_{it} at $E = E_c - 0.2$ eV for the cases of NO10, NO120 and Thermal+NO. The black diamonds represent the results of our previous work when nitridation was performed on thermal oxides under various N_2 + O_2 annealing conditions [3]. (b) Schematics of the carbon byproduct desorption during direct NO nitridation and NO annealing. (c) Relationship between direct NO oxynitridation time and the ratio of the oxidation rate to the nitridation rate(r_{ox}/r_{nit}). r_{ox}/r_{nit} was defined as the ratio of the average rate of change of $T_{SiO(N)}$ to that of A_N shown in Fig. 2.

Impact of Substrate-Surface Oxidation Treatment and Post-Deposition Annealing on β-Ga_2O_3 (001) MOS Interfaces with ALD-Deposited Al_2O_3 and SiO_2

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1. Introduction

β-Ga_2O_3 is expected as a next-generation power device material due to its large bandgap (4.5 eV) and a high breakdown electric field. Its MOS interface characteristics are expected to be influenced significantly by employed gate dielectric materials and their post-deposition annealing (PDA) conditions. For the case of using a SiO_2 film as a dielectric, it has been pointed out that high temperature annealing under an oxygen ambient is essential for reducing the interface state density (D_{it}) [1,2]. This indicates the necessity of oxygen vacancy removal from the interface region, especially the surface region of Ga_2O_3. On the other hand, oxide semiconductors in general have unique characteristics in that oxygen vacancies have important role in electron conduction, so an excessive oxidation at high temperature that reduces oxygen vacancies in the bulk part of Ga_2O_3 substrate should be avoided. Actually, such an oxidation process is reported to result in a significant reduction in carrier concentration of β-Ga_2O_3 [2,3]. Therefore, selective oxidation of the substrate surface without influencing the bulk property by high-temperature oxidation is demanded. Then the atomic layer deposition (ALD) method will be beneficial because it allows us to control the strength of interface oxidation by choosing oxidants, which potentially enables such a selective oxidation of the substrate surface. Furthermore, to form an interface with good electrical properties, it is expected that the interface of the insulating film side must also be sufficiently relaxed, thereby suppressing defect formation. In this study, we investigated the reduction of D_{it} caused by O_3 surface oxidation prior to film deposition and the type of oxidants (O_3, H_2O) during ALD film deposition when employing Al_2O_3 and SiO_2 as gate dielectric layer, together with the influence of post-deposition annealing (PDA) conditions.

2. Experimental

β-Ga_2O_3 (001) substrates with n-type epitaxial layer ($N_D \sim 1\times10^{16}$ cm^{-3}) were cleaned by HF, followed by Al_2O_3 deposition as the gate dielectric by ALD using trimethylaluminum as a precursor. The oxidant in ALD for sample (A) and (B) was H_2O, while that for sample (C) was O_3. Only for samples (B) and (C), the surface oxidation treatment by O_3 at 300°C as illustrated in inset of Fig.1(b) was employed. After PDA at 600°C for 5 min under O_2 ambient, Au on top and Ti/Au on the back were deposited to fabricate MOS capacitors. Various PDA conditions were examined for the film deposited by O_3-ALD after the surface oxidation treatment, sample (D): O_2, 600°C, 60 min; (E): 0.1% O_2 + N_2, 600°C, 60 min; and (F): O_2, 1000°C, 5 min. The MOS capacitors of SiO_2 gate dielectrics were also fabricated by ALD deposition with tris(dimethylamino)silane as the precursor and O_2 plasma as the oxidant, followed by PDA under an O_2 ambient at (G): 600°C, 60 min, (H): 1000°C, 5 min.

3. Results and Discussion

Bidirectional C-V characteristics of sample (B) are shown in Fig. 1(a). The use of O_3 as an oxidant and surface oxidation was found beneficial to improve the characteristics compared to H_2O (sample (A)). Note that the use of O_3 is advantageous for reducing oxygen deficiency near the surface region of Ga_2O_3 even at low temperature (300°C). Figure 1(b) shows that energy distribution of D_{it} of sample (A)~(C) evaluated by the conductance method. Compared to sample (A), sample (B) and (C) exhibited a reduction in D_{it} of approximately one order of magnitude, indicating that surface oxidation by O_3 of Ga_2O_3 substrate decrease D_{it} by filling the oxygen vacancies on the surface as expected [4], though a significant amount of negative fixed charges were observed, which indicates a necessity of further improvement of ALD or PDA conditions.

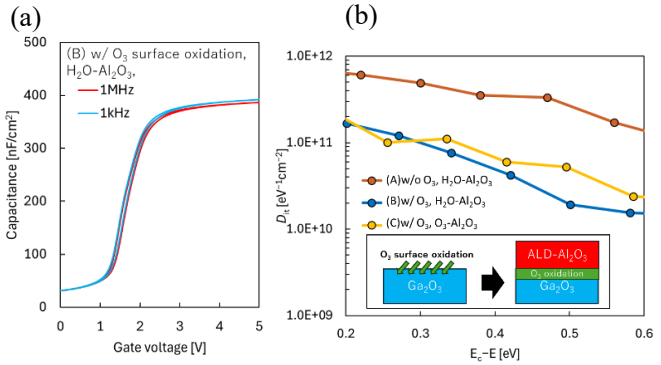

Fig. 1(a) Bidirectional C-V characteristics of sample (B) H_2O-Al_2O_3 with O_3 surface oxidation treatment, (b)Energy distribution of D_{it} for sample (A)~(C).

Next, we examined the effects of PDA conditions on the samples of O_3-ALD Al_2O_3 with the prior O_3 surface oxidation

treatment. Figure 2(b) shows the energy distribution of D_{it} for samples (C)~(F). Either by employing higher PDA temperature (sample C) or extending PDA duration to 60 min at 600 (sample D) improves D_{it}, thanks to a thermal budged. However, it should be noted that by using an annealing gas of 0.1% O_2+N_2 (F), even at a low PDA temperature of 600°C, D_{it} was reduced to ~ 2×10^{10} $eV^{-1}cm^{-2}$ which was even below that obtained with 1000°C PDA.

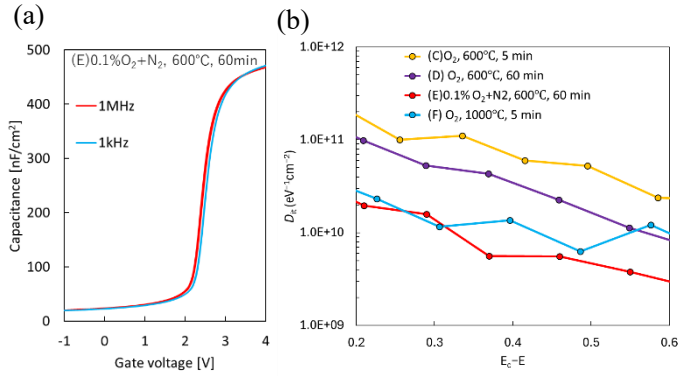

Fig.2 (a) C-V characteristics of sample (E), (b) Energy distribution of D_{it} for the sample with various PDA conditions (sample (C)~(F)).

In Fig. 3(a) the values of D_{it} @E = E_c−0.2 eV under various PDA conditions are compared for both O_3-ALD Al_2O_3 cases and plasma O_2-ALD SiO_2 cases. For Al_2O_3 samples, either the increase in PDA temperature or extension in PDA duration tends to decrease D_{it}. This trend is thought to be due to the fact that higher thermal budget is preferred for the relaxation of the Al_2O_3/Ga_2O_3 interface structure. When PDA was performed with 0.1% O_2+N_2, such structural relaxation of the interface would achieve more efficiently, even at 600°C. The low oxygen partial pressure PDA would be beneficial to reduce the excess oxygen which might prohibit the relaxation of the interface structure. In the O_3-ALD process with the prior surface oxidation treatment, the repetitive O_3-oxidation should be beneficial for oxygen deficiency annihilation on Ga_2O_3 surface as discussed above, but excess oxidation would work disadvantageous in terms of structural relaxation at the interface. For the plasma-ALD SiO_2 samples (samples (G) and (H)), D_{it} reduction down to approximately 1×10^{11} $eV^{-1}cm^{-2}$ was achieved but it was not as low as that for the O_3-Al_2O_3 sample, probably due to the unoptimized deposition process conditions. Figure 3(b) compares the hysteresis width normalized by capacitance equivalent thickness for the samples with various PDA conditions. Overall trend seems similar with that for D_{it} shown in (a). However, for Al_2O_3 samples, employing high temperatures is not efficiently work to suppress the near-interface traps in Al_2O_3. Actually, an increase of oxide traps due to Ga diffusion into Al_2O_3 above 700°C has been reported [5]. For sample (E), not only D_{it} but the hysteresis width is also well suppressed probably because of the moderate PDA temperature of 600°C. On the other hand, the SiO_2/Ga_2O_3 interface is known to be thermodynamically stable even at high temperature [6], and the hysteresis width of the plasma-SiO_2 sample was dramatically improved by increasing the PDA temperature to 1000°C.

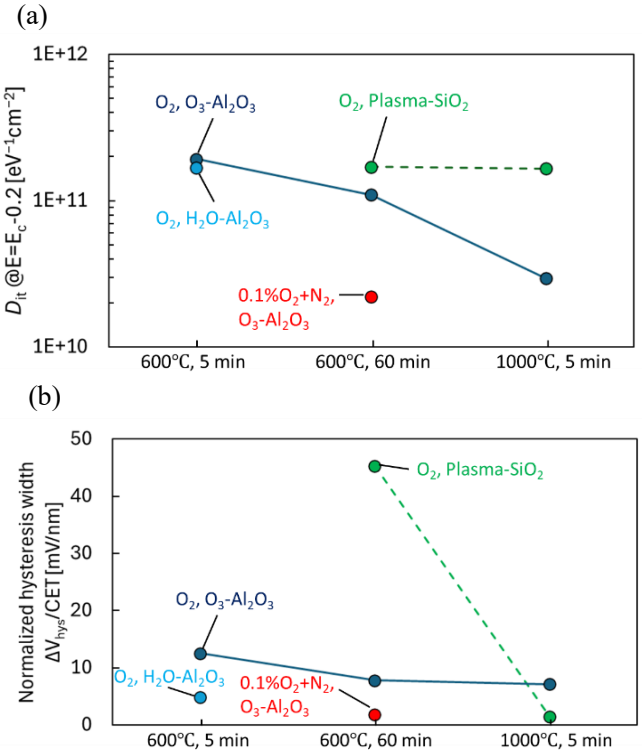

Fig.3, (a)D_{it} @E=E_c−0.2, (b) Hysteresis width normalized by capacitance equivalent thickness of Al_2O_3/β-Ga_2O_3 and SiO_2/β-Ga_2O_3 MOS capacitors were compared for various PDA conditions.

4. Conclusion

β-Ga_2O_3 (001) MOS interface characteristics with low D_{it} and small C-V hysteresis were successfully demonstrated by employing ALD-deposited Al_2O_3 and SiO_2 as gate dielectrics. For Al_2O_3 stacks, combining the substrate surface oxidation treatment with O_3 with the ALD using O_3 as the oxidant works efficiently to reduce D_{it} down to ~2×10^{10} $eV^{-1}cm^{-2}$ even with a relatively low temperature PDA at 600°C, especially when an ambient with reduced oxygen partial pressure, such as 0.1% O_2, was employed as the PDA ambient.

Acknowledgement

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Recent progress in ultra-wide bandgap oxides: GeO_2 for power devices and Ga_2O_3 for metamaterials

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Ultra-wide bandgap (UWBG) oxides are being researched as a next-generation material for electronic or optical applications, leveraging its large bandgap. Among these, rutile type germanium dioxide (r-GeO_2) is attracting attention as a new power semiconductor due to its huge bandgap of 4.74 eV [1] and the potential for both p-type and n-type carrier control by doping technique [2]. However, r-GeO_2 has been quite difficult to grow for two reasons [3]. The first reason is that the formation free energies of the α-quartz phase, the amorphous phase, and the rutile phase–the crystalline polymorphs of GeO_2–are very close. This made it difficult to distinguish between these three phases and grow only the rutile phase. The second reason is that r-GeO_2 is a highly volatile material during crystal growth. It has been reported that during crystal growth, GeO_2 combines with metallic germanium, forms the gaseous compound GeO, and then migrates within the crystal before evaporating [4]. Crystal growth of r-GeO_2 bulk has been reported using the flux [5-7], the Czochralski [8] and TSSG method [9]; however, due to their tendency to evaporate during growth, the obtained crystals are small, typically ranging from 5 mm to 15 mm in size. A similar trend was observed in thin film growth, with early reports by MBE [3], PLD [10], and mist CVD [11] indicating extremely low growth rates due to re-evaporation or the presence of amorphous phases. Recent studies indicate that such issues are being resolved through methods such as MOCVD [12,13] and mist CVD [14] with buffer layers.

Ga_2O_3 exhibits five crystalline polymorphs, among which the thermally most stable β phase and the metastable α phase have been reserched as power semiconductor materials [15][16]. However, since both α and β Ga_2O_3 do not exhibit band-edge luminescence, their application in light-emitting devices is difficult. Meanwhile, new applied research on Ga_2O_3 is beginning. α-Ga_2O_3 possesses nine distinct crystals with the same corundum structure[17]. Among these, certain combinations feature closely matched lattice constants and large refractive index differences. By arranging these into a layered structure, it is possible to create novel metamaterials that transmit specific wavelengths while reflecting light in other wavelength regions. Unlike conventional bandpass filters or DBRs, a key feature of this approach is its ability to reflect all wavelengths except the targeted ones. One such combination is α-Ga_2O_3 and α-Fe_2O_3. This combination transmits the 3μm light emitted from the heat source while reflecting other wavelengths back to the heat source for reuse in reheating [18]. By applying this new metamaterial multilayer, it is possible to significantly improve the drying and heating efficiency of large-scale equipment such as solar cells and fuel cells.

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	β-Ga_2O_3	**α-Ga_2O_3**	**GeO_2**
Band gap [eV]	4,6-4.9	5.3-5.7	4.74(film)-5.5(bulk)
Electron/Hole mobility [cm^2/Vs]	150/- (Experimental value)	100/- (Experimental value)	377/29 (calculation)
Thermal conductivity [W/m·K] R.T.	10.9-27.0	8.94-11.61 (calculation)	52
Compounds with the same crystal structure	-	α-X_2O_3 (X=Al, In, Fe, Cr, V, Ti, Rh,Ir)	XO_2 (X=Si,Sn,Ti, etc..)

Fig.1 Comparative physical properties of β-Ga_2O_3, α-Ga_2O_3, and r-GeO_2.

Power Device & Processes | Electron device, process, and characterization

Fri. Nov 7, 2025 3:25 PM - 4:25 PM JST | Fri. Nov 7, 2025 6:25 AM - 7:25 AM UTC 5F-Meeting Room

[S7] Power Device & Processes (2)

Chair:Motoyuki Sato(Tokyo Electron), Toshinori Numata(Toyota Technological Institute)

3:25 PM - 3:55 PM JST | 6:25 AM - 6:55 AM UTC

[S7-01]

Effects of Nitrogen Doping on Electrical Properties of Ga_2O_3

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3:55 PM - 4:25 PM JST | 6:55 AM - 7:25 AM UTC

[S7-02]

Unique techniques of ALD for semiconductor devices

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Effects of Nitrogen Doping on Electrical Properties of Ga_2O_3

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1. Introduction

It is well known that nitrogen (N) atoms function as deep acceptors in Ga_2O_3 [1, 2]. We first demonstrated N doping by ion implantation [3]; however, the technique also provides damage and defects into the Ga_2O_3 crystal. Furthermore, the high-temperature activation annealing at 1100°C causes surface charge depletion due to Ga atom desorption. To avoid the issues, development of epitaxial N doping technology is highly demanded.

In this talk, we will first present the effect of N radical irradiation, which provides high-density N doping into the region near the surface, on electrical properties of Ga_2O_3 Schottky barrier diodes (SBDs). Then, electrical properties of N-doped Ga_2O_3 thin films grown by molecular beam epitaxy (MBE) will be discussed [4].

2. Experimental Procedure

The N radical irradiation to Ga_2O_3 (100) and (010) substrates was simultaneously performed in an MBE growth chamber for 120 min as shown in Fig. 1(a). The RF power of the N plasma cell was 500 W, the N_2 flow rate was 0.6 sccm, and the substrate temperature was 700°C. SBDs were fabricated on the Ga_2O_3 substrates with the nitrided surfaces by the process flow as shown in Fig. 1(b).

The epitaxial N doping into Ga_2O_3 thin films was performed by simultaneously supplying O and N radicals during MBE growth. For the growth, the RF powers of the O and N plasma cells were set at 250 and 350 W, and the O_2 and N_2 flow rates were 2.0 and 0.6 sccm, respectively. The substrate temperature was 620°C.

3. Results and Discussion

Significant improvements in device characteristics of the Ga_2O_3 SBDs were obtained by means of the N radical irradiation before fabrication of anode electrodes, such as disappearance of kinks in the current-voltage characteristics and improvement in in-plane uniformities of the electrical properties (see Fig. 2).

We succeeded in controlling doped N densities in a wide range over five orders of magnitude ($N = 10^{17} – 10^{21}$ cm^{-3}) (see Fig. 3). Structural properties of the N-doped Ga_2O_3 films kept being decent and were comparable with those of unintentionally doped Ga_2O_3 ones grown by MBE at the same condition. It was confirmed from the electrical properties that the doped N atoms functioned as deep acceptors and compensated the background donors.

4. Conclusions

We developed two N doping techniques for Ga_2O_3 and found that the doped N atoms were electrically active acting as deep acceptors to compensate the background donors.

Acknowledgements

This work was supported by MIC under a grant entitled “R&D of ICT Priority Technology (JPMI00316): Next-Generation Energy-Efficient Semiconductor Development and Demonstration Project (first and second periods) (in collaboration with MOEJ).

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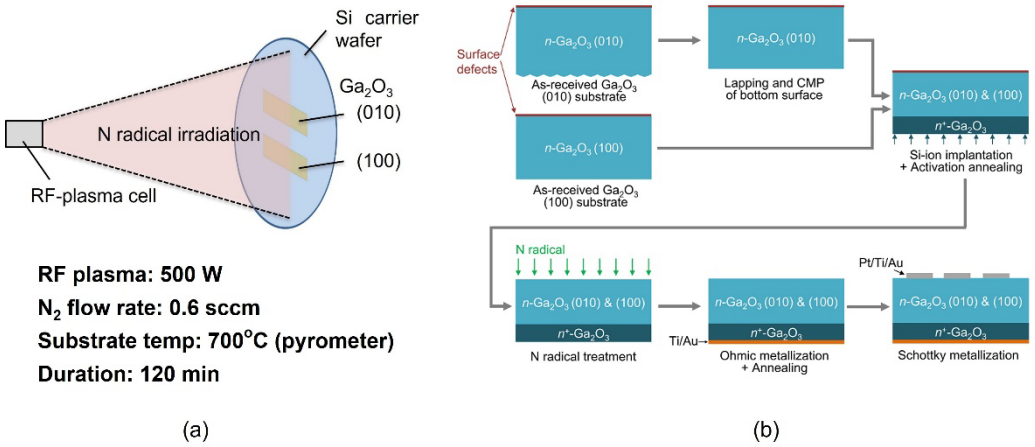

Fig. 1 (a) Schematic of N radical irradiation process in MBE chamber. (b) SBD fabrication process flow.

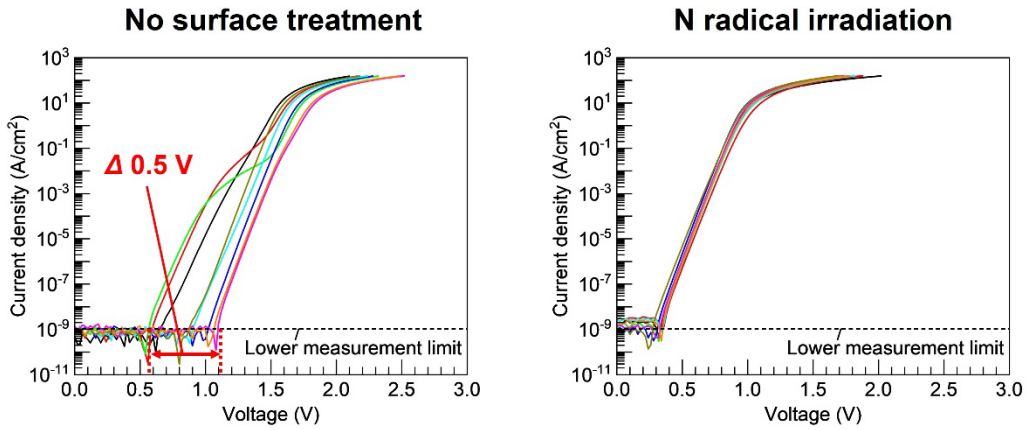

Fig. 2 Comparison of forward current–voltage characteristics of SBDs fabricated on Ga_2O_3 (100) substrates without and with N radical irradiation.

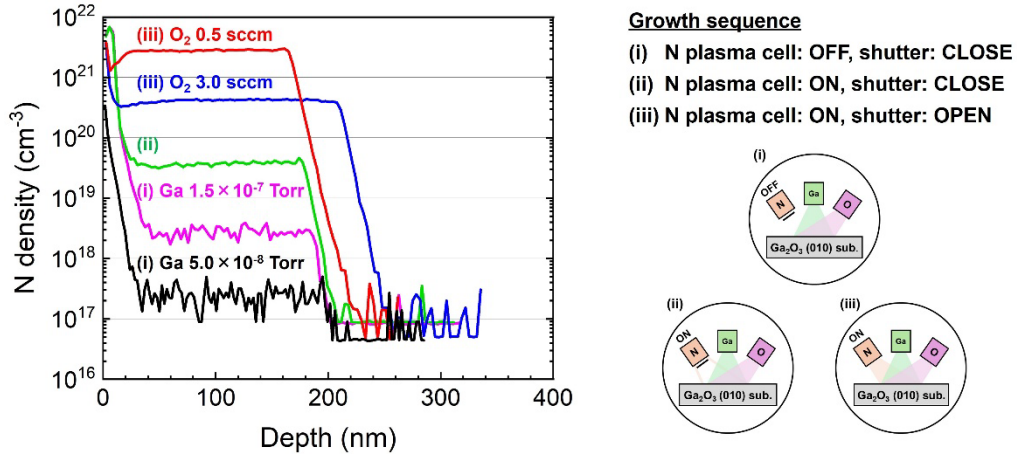

Fig. 3 Depth profiles of N densities in MBE-grown N-doped Ga_2O_3 thin films analyzed by secondary ion mass spectrometry.

Unique techniques of ALD for semiconductor devices

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1. Introduction

Atomic layer deposition (ALD) technique is the optimal approach to fabricating conformal films on three-dimensional structures for semiconductor devices such as GaN and Ga_2O_3 power devices, metal/high-k CMOS, oxide-semiconductor FET, DRAM, and FeRAM. ALD sequence generally consist of four steps: (a) Adsorption of precursor gas on the substrate, (b) Ar purge gas to exhaust residual precursor gas into chamber, (c) Reactant gas (H_2O, O_3, O-plasma, NH_3, N-Plasma, etc.) to form target films (oxide, nitride, etc.) on substrate, (d) Ar purge gas to exhaust residual reactant gas into chamber. The four steps constitute one ALD cycle, and the growth rate is expressed as GPC. The GPC which depends on the precursor, ranges 0.03~0.2 nm/cycle. Until now, numerous studies have been conducted using the unique features of ALD. In this paper, I introduce several topics such as dipole control by ALD cycles for metal/high-k CMOS, selective adsorption of TDMAS precursor on HfO_2 underlayer, and GaN surface modification by ALD-dummy-SiO_2 technique, mainly obtained in the author's group.

2. Dipole control by ALD cycle for metal/High-k CMOS

ALD became popular with the HfO_2 film deposition as gate insulator of metal/high-k CMOS in around 2000 year. Metal/high-k CMOS is currently based on the GAA structure as shown in **Fig. 1**. To control V_{th}, the insertion of dipole layer between the HfO_2 and SiO_2 interfacial layer and WFM layer between the HfO_2 and TiN gate electrode is being studied. La_2O_3, Y_2O_3, and Al_2O_3 have been mainly investigated as dipole layers for n- and p-MOSFETs, respectively [1,2]. It has been reported that V_{th} can be easily controlled by each ALD cycle. WFM was also fabricated using the ALD method by doping TiN with elements such as Al and O.

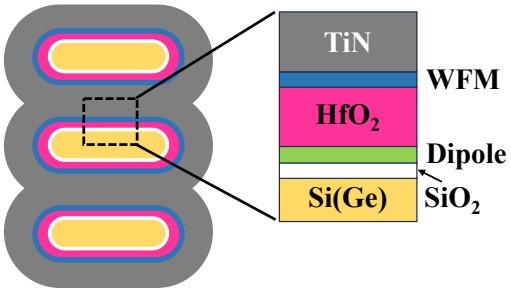

Fig. 1. Schematics of GAA (Gate-All-Around) structure with dipole and WFM layers.

3. Selective adsorption of TDMAS precursor on HfO_2 underlayer

GaN MOS devices with amorphous $HfSiO_x$, $AlSiO_x$ and $HfAlO_x$ gate insulators have been widely investigated as a means of obtaining superior device performance such as high g_m and low leakage current [3,4]. $HfSiO_x$ film was generally formed from the $(HfO_2)_m/(SiO_2)_n$ laminate. Therefore, accurate GPC of the SiO_2 layer deposited via ALD with TDMAS ($SiH(N(CH_3)_2)_3$) precursor on the HfO_2 layer was required. The GPC (0.22 nm/cycle) of ALD-SiO_2 film on HfO_2 underlayer significantly increased compared to that on SiO_2 underlayer (0.043nm/cycle) [5]. To understand this behaviour, we studied the GPC of ALD-SiO_2 on various metal-oxide (M-O) underlayer. Surprisingly, the GPC of the ALD-SiO_2 film increased in the following order: $HfO_2 > TiO_2 > Al_2O_3 > SiO_2 > Ga_2O_3$. Furthermore, we found a correlation between the GPC of the ALD-SiO_2 film and the difference in the electronegativity of the M-O underlayer as shown in **Fig. 2**. Considering to ALD-SiO_2 growth mechanism, the Si atom which has a low positive charge, of the TDMAS precursor is selectively adsorbed toward the O atoms which has a high negative charge, of the M-O underlayer. As a results, a large amount of the TDMAS precursor adsorbed on HfO_2 unerlayer and led to high GPC. Based on these experimental data, we were able to fabricate the targeted Hf/Si ratio in the $(HfO_2)_m/(SiO_2)_n$ laminate.

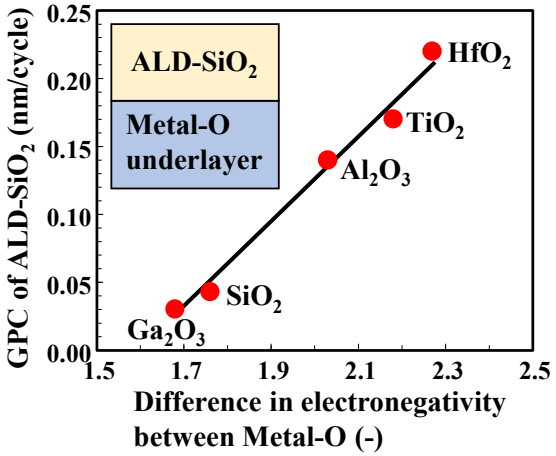

Fig. 2. Correlation between the GPC of the ALD-SiO_2 film and the difference in the electronegativity of M-O.

4. GaN surface modification by ALD-dummy-SiO_2 technique

In GaN MOS capacitors, there is a native oxide (GaO_x) film grown epitaxially on the GaN surface, which act as an electrically unstable GaO_x layer [6]. To modify the unstable GaO_x layer on GaN surface, we proposed ALD-dummy-SiO_2 technique, which is a unique and simple process as shown in **Fig. 3** [7,8]. ALD-dummy-SiO_2 layer (5 nm) was deposited on GaN and subsequently annealed at 800 °C in N_2. The ALD-dummy-SiO_2 layer was removed with BHF solution. Next, a 10-nm-thick Al_2O_3 insulator was deposited on the modified GaN substrate via ALD at 300 °C. Finally, Pt gate electrode and Ti/Pt ohmic contact were formed to fabricate n-GaN/Al_2O_3/Pt capacitor (ALD-dummy-SiO_2). A n-GaN/Al_2O_3/Pt capacitor was also prepared without the ALD-dummy-SiO_2 process as reference (Standard). **Figure 4** shows the V_{fb} shift as a function of bias V-V_{fb} of the ALD-dummy-SiO_2 and Standard capacitors under positive bias stress. The V_{fb} shift of the ALD-dummy-SiO_2 significantly reduced compared to that of the Standard. This is because the unstable GaO_x layer was removed and oxygen-ordered GaO_x layer was formed on the surface of GaN [9]. As a result, the modified GaN led to superior characteristics such as a small V_{fb} shift under PBS.

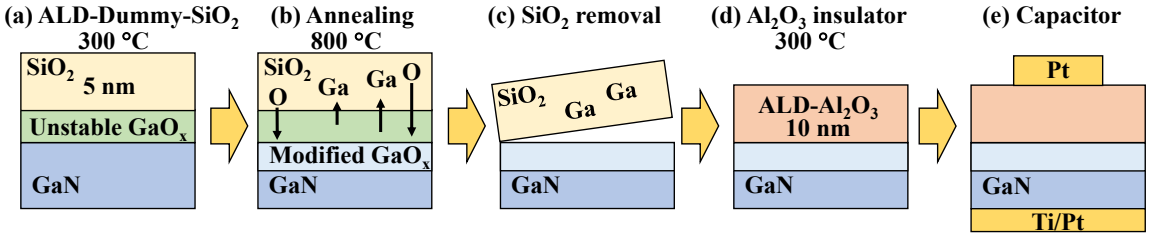

Fig. 3. Schematics of GaN surface modification and capacitor fabrication by ALD-dummy-SiO_2 technique.

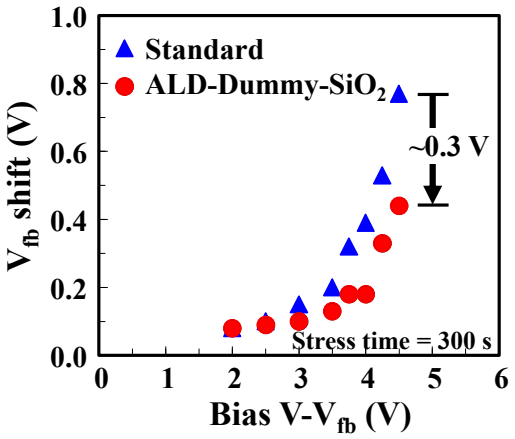

Fig. 4. The V_{fb} shift as a function of bias V-V_{fb} of the ALD-dummy-SiO_2 and Standard capacitors under PBS.

I concluded that ALD is not the use as the equipment, but rather the utilization of its unique characteristics.

Acknowledgements

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Closing

Fri. Nov 7, 2025 4:25 PM - 4:50 PM JST | Fri. Nov 7, 2025 7:25 AM - 7:50 AM UTC 5F-Meeting Room

[CS] Closing

Chair:Masao Inoue(Renesas Electronics), Mitsuru Sometani(National Institute of Advanced Industrial Science and Technology (AIST))

4:25 PM - 4:50 PM JST | 7:25 AM - 7:50 AM UTC

Award Celebration & Closing Remarks