Performance Improvement of n-channel TFT on Solid-Phase Crystallized poly-Ge by Channel Width Shrinking

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【**Introduction**】Our group succeeded in the synthesis of high-quality polycrystalline (poly-) Ge thin films using the advanced solid-phase crystallization (SPC) technique on glass and demonstrated accumulation mode p-channel TFT on the SPC-Ge [1-3]. Recently, we have also demonstrated n-channel TFT to realize a CMOS circuit on our SPC-Ge. However, its performance has room for improvement, notably its ON/OFF ratio [4]. In this paper, we introduce the shrunk channel width design to our inversion mode n-TFT on poly-Ge. By comparing with conventional channel structure, it shows a positive effect on the ON/OFF ratio of n-channel poly-Ge TFT.

【**Fabrication process and approach to reduce OFF current by channel-shrinking**】Figure 1 shows the fabrication process of inversion mode n-channel TFT. Based on these process, we aimed to decrease the off-state leakage current by shrinking the channel width. Figure 1 also shows the 3D structure and the optical microscope photo of the conventional and dumbbell-shaped channel TFT island pattern. We formed those two types of island shape TFTs on the same chip, so that we can easily compare just the difference of the island shape.

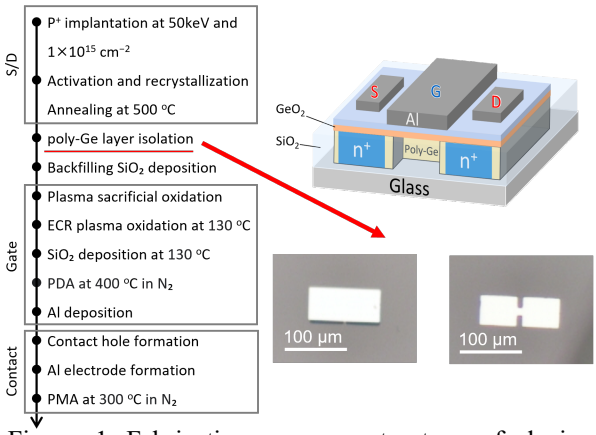

Figure 1 Fabrication process, structure of device illustration, and top-view island shapes (conventional rectangle and new dumbbell shape).

【**Results and discussion**】 Figure 2 shows I_D-V_G transfer characteristics of the fabricated inversion mode n-channel TFT. Here, the channel length was fixed 10 μm. The channel widths of conventional and dumbbell-shaped devices are 25 μm and 7 μm, respectively. By comparing the I_D-V_G with those two types of channel shape, we can see channel shrinking has an positive effect on the improvement of the ON/OFF ratio, particularly OFF current reduction. Figure 3(a) and 3(b) show the maximum and minimum of the I_D. Here, the channel length is 7 μm, and the V_D is 0.1V. It is clear to see that, the maximum of I_D increases with the increasing channel width, and both two types of channel shape show the same trend. It can be naturally understood. However, it shows apparently decrease in the minimum of the I_D, which is independent of the channel width. This means the channel width shrinking mainly affected the off current reduction on the channel region, and it did a great influence on increasing the ON/OFF ratio from 10 level to 100 level.

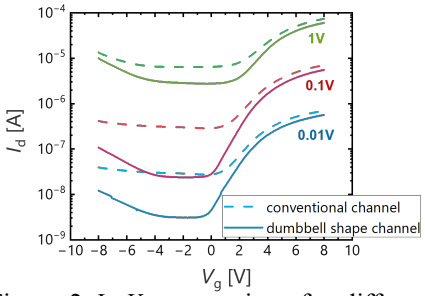

Figure 2 I_D-V_G comparison for different island shapes with the same channel length.

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【**References**】[1] K. Toko *et al.*, Sci. Rep. 7, 16981 (2017). [2] T. Imajo *et al.*, ACS Appl. Electron. Mater. 4, 269 (2022). [3] K. Moto *et al.*, Appl. Phys. Lett. 114, 112110 (2019). [4] L. Huang *et al.*, J. Appl. Phys. 63, 02SP42 (2024).

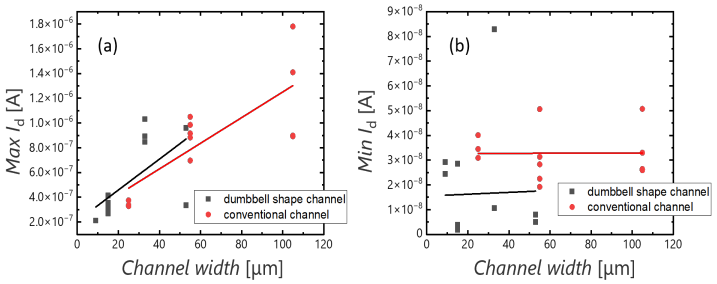

Figure 3 (a) max and (b) min I_D comparison for different island shapes with the same channel length L = 7 μm.