Modeling and Evaluation of a Power Management System for RISC-V-Based Digital Platforms

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Introduction

As digital platforms continue to grow in complexity and capability, there is a growing need for sophisticated power management units (PMUs). This is especially true for systems leveraging RISC-V CPUs, which allows for flexibility due to its open-source nature [1].

Despite the advantages offered by RISC-V CPUs such as their customizability, there are significant challenges in optimizing power consumption without compromising performance [2].

This paper focuses on the development of the PMU design for RISC-V based digital platform. By integrating power gating and staggering the powering of the modules, it would allow for greater efficiency as only the necessary modules are powered, and the power gating minimizes power draw.

PMU Overview

The PMU powers each module sequentially, waiting for a return signal before proceeding. As seen in Fig. 1 it starts by powering the sensor and ADC unit. Once conversion is done, it powers the RISC-V CPU to process the data. After processing, the external memory is powered to record the data, while the sensor and ADC are powered down. Finally, the CPU is powered down, and the RF circuit operates, feeding data from the external memory at 1 MHz.

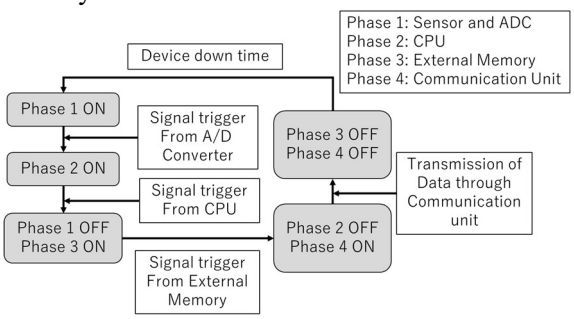

Fig. 1 Diagram of the Process of the PMU

Results and Discussion

In Fig. 3(a) the experimental setup for the test can be seen. The PMU is connected to a simple power gate which powers the different modules.

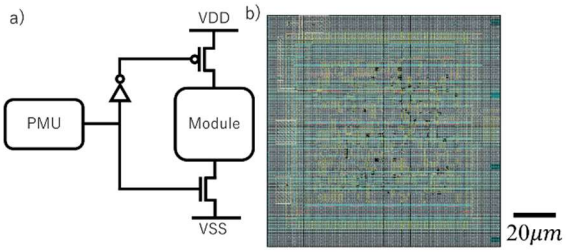

Fig. 3 (a) Setup of the PMU with power gating and (b) the layout of the PMU

This would help isolate the modules from VDD and GND while it is not operational reducing power consumption while it is at rest and easy operation from the PMU. We have tested the power gate with the RISC-V CPU and RF circuit operation and have confirmed its operation.

In Fig. 3(b) The layout of the PMU with a size of $110 \times 110\ \mu m^2$, which has been processed through Design Vision and ICC Compiler can be seen.

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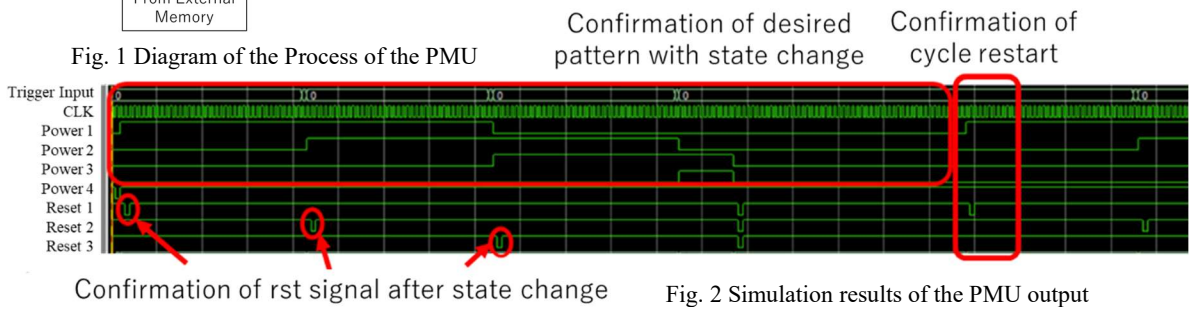

Fig. 2 Simulation results of the PMU output