多接合 p-on-n 太陽電池に適用可能なウェーハ接合界面の電気的特性
Electrical properties of wafer-bonded interfaces applicable for multijunction p-on-n solar cells

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1 Introduction

At the last spring meeting, we reported the successful fabrication of multi-junction solar cells (MJSCs) with a p-on-n configuration using a direct wafer bonding technique [1]. Subcells grown separately on InP and GaAs wafers were bonded together utilizing a heavily doped n-GaAs//n-InGaAs/p-InGaAs structure, where the notation // indicates the bonding interface. This structure resulted in a voltage loss of approximately 0.1 V under 1-sun operation. To enhance the performance of wafer-bonded p-on-n MJSCs, we investigated the electrical characteristics of bonded interfaces between various applicable material combinations in this work.

2 Experimental details, results and discussion

We investigated eight bonding combinations, including n-GaAs//p-InP, n-InGaP//p-InP, n-GaAs//p-InGaAs, n-InGaP//p-InGaAs, n-GaAs//n-InGaAs/p-InGaAs, n-InGaP//n-InGaAs/p-InGaAs, n-InGaP/p-AlGaAs//p-InGaAs, and n-InGaP/p-AlGaAs/p-InAlGaP//p-InGaAs. The surface activated bonding technique was employed with optimized parameters: 1 minute of surface activation followed by 5 minutes of bonding under a pressure of 15 kN. Rapid thermal annealing (RTA) was used to anneal the bonded samples. Subsequently, GaAs wafers were selectively removed, and metal electrodes were deposited on both sides, with a front pattern of 0.04 cm² arrays, which were later electrically isolated using high mesa etching. Figure 1 depicts the sample structure having the n-GaAs//p-InGaAs interface.

Initially, it was observed that two combinations involving p-InP exhibited weak bonding strength, allowing the bonded samples to be easily separated with minimal force. Consequently, this hindered the GaAs wafer removal process. Among the remaining six combinations, rectified I-V characteristics were observed, each with distinct turn-on voltages corresponding to the choice of materials. Post-annealing at 450-550°C for 5 minutes proved effective in enhancing the ohmic properties of the bonded interfaces. However, annealing at 600°C resulted in the formation of cracks and line defects along the [011] direction in thin films deposited on the GaAs side, leading to degraded I-V characteristics. The I-V results from the n-GaAs//p-InGaAs sample are illustrated in Fig. 2, with additional findings to be presented during the upcoming meeting, including their potential applications in practical MJSCs.

3 Summary

We explored several bonding combinations suitable for p-on-n MJSCs. Post-annealing was essential to enhance the I-V characteristics of the bonded interfaces, although it could also introduce line defects that degrade electrical performance.

[1] H. Sodabanlu et al, 71st JSAP Meeting, 23a-12L-1.

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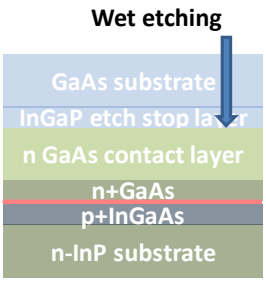

Fig. 1 Schematic of n-GaAs//p-InGaAs sample

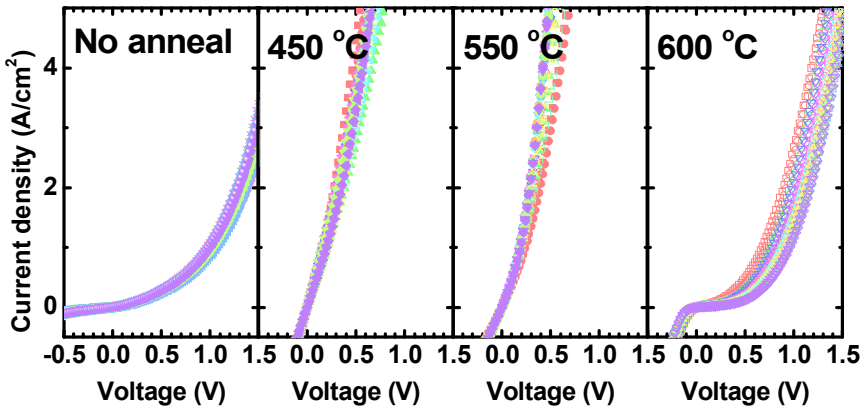

Fig. 2 I-V characteristics of n-GaAs//p-InGaAs sample without and with post annealing