SiC Formation on SiNW and Si Surface via Close Space Technique Carbonization

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Introduction

Silicon carbide (SiC) has emerged as a promising wide-bandgap semiconductor for next-generation power and high-frequency electronics, owing to its large bandgap (3.26 eV for 4H-SiC), high thermal conductivity (3.7 W cm^{-1} K^{-1}), excellent chemical stability, and high breakdown field strength. However, the heteroepitaxial growth of high-quality, continuous SiC thin films on silicon (Si) substrates remains a critical challenge. Under low-pressure conditions, rapid gas-phase reactions between CH_4, Si, and residual oxygen at elevated temperatures complicate process control, while Ar carrier gas can promote unwanted Si transport. To overcome these limitations, we introduce a modified close space technique (CST) that confines CH_4/Ar flow between two boundary layers, suppressing undesired gas-phase reactions [1].

Experimental section

Silicon (Si) with a carbon (C) layer formed by carbonization at 1000 °C, along with Si nanowire (NW) samples of uniform height (600 nm) fabricated via electron beam lithography and Bosch etching, were initially subjected to CST carburization at 1200 °C (Fig. 1) for 1, 15, and 30 minutes, as shown in Fig. 2. Subsequently, SiNWs with different heights ranging from 600 nm to 2400 nm were carburized under the same CST conditions at 1200 °C for 15 minutes (Fig. 3). These experiments, involving variations in carbonization duration and the spatial gap between the carbonized Si layer and the SiNW or Si surface, were carefully monitored to enable the effective formation of a SiC layer.

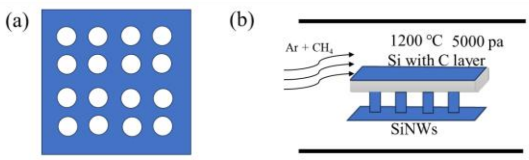

Figure 1. (a) Top-view schematic of the SiNW substrate. (b) Schematic illustration of the sample placement during the carburization process.

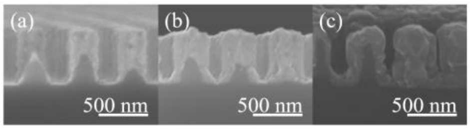

Figure 2. Cross-sectional SEM images of SiC/SiNW samples after annealing at 1200° C for (a) 1 min, (b) 15 min, and (c) 30 min, respectively.

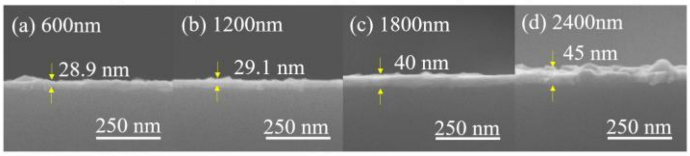

Figure 3. (a-d) Cross-sectional SEM images of SiC/Si surfaces formed by different inter-wafer gap, showing the corresponding SiC layer thickness after carburization.

Results and discussion

Under the CST method, the growth rate of SiC on SiNWs and Si surfaces was significantly reduced with shorter carburization durations and smaller inter-wafer gaps, as shown in Figs. 2 and 3. A growth rate of approximately 1.33 nm/min was observed for SiC on SiNW surfaces. Notably, Si surfaces without elevated NW support structures, corresponding to an approximate 1 µm height difference, exhibited a measurable increase in SiC thickness. This increase, approximately 10 nm of additional SiC per micron of height, suggests a strong correlation between vertical confinement and localized growth enhancement. The internal geometry and spacing between facing wafers play a critical role in shaping the local reaction environment by suppressing gas-phase diffusion and promoting vapor-solid or solid-solid interactions. The confined configuration retains reactive species near the substrate surface, thereby minimizing undesired side reactions. Conversely, increasing the inter-wafer spacing reduces the confinement effect, potentially disturbing local concentration gradients and altering surface reaction kinetics. This phenomenon will be the focus of future optimization efforts aimed at further elucidating the spatially confined reaction dynamics governing CST-based SiC formation.

Reference

1. T. Furusho, S.K. Lilov, S. Ohshima, and S. Nishino, Thirteen. Int. Conf. Cryst. Growth Conj Unction Elev. 237-239, 1235-1238 (2002).