On-Current Variability Components in 65nm Bulk and FDSOI MOSFETs at Cryogenic Temperature

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[Introduction] Variability decomposition is a very powerful tool to understand the variability characteristics of the devices, albeit with quite some limitations. The room temperature variability decomposition results have already been discussed [1]. In this work, we carried out variability decomposition for cryogenic bulk and FDSOI devices. **[Fabrication]** The number of both bulk and FDSOI devices is 256, and the devices are prepared using 65nm process node with W/L=140nm/60nm. Cryogenic Temperature (CT) is set to be 1.5K for both device types, while the room temperature (RT) is set to be 300K. **[Results and Discussion]** Analysis is limited to the saturation region as the linear region operation features unideal and increased variability [2]. Previous works decomposed variability into threshold voltage (Vthc), current onset voltage (COV), and transconductance (Gm) factor. However, Gm factor, or rather the extrapolated threshold voltage, in the saturation region is not consistently obtainable with great confidence. Therefore, the scheme from [1] must be modified. As also shown in Fig. 1, Pelgrom plots indicated that the definition of threshold voltage is also a very important issue. The traditional definition of Vthc at 1e-7 A/normalized, while being fine at RT, is suffering from non-random variability at CT as indicated by the Pelgrom plot. This is probably caused by the reduced thermal excitation at CT, since Vthc essentially reflects the critical channel potential, and its fluctuation is averaged out to a certain extent at RT. Reduced thermal energy thus makes the carriers unable to jump out of the potential well and thus showing non-random/non-averaged variability. The new scheme is therefore considered to comprise only a Vthc and a Gm factor, while the Vthc is now extracted at 1e-5 A/normalized. The immediate RT and CT decomposition results are shown as in Fig. 2. After removing outlier variability, both devices still see increased variability at CT. In bulk FETs, Vthc variability is dominant and much higher than SOI due to RDF. For SOI, the difference of variability between Vthc and Gm is limited, especially in CT. FDSOI's relatively more significant Gm impact as compared to bulk may be caused by reduced RDF shadowing at CT and higher vulnerability to freeze out [3-4]. The increase of Gm impact of both devices at CT is also considered to be related to freezeout that happens in both devices. **[Conclusion]** A new variability decomposition scheme is proposed, and it is found that even under CT, Gm's impact is still important for FDSOI and Vthc's impact is more important for bulk FETs. **[References]** [1] Z. Liu et al., JJAP 61, 2022. [2] Z. Liu et al., JJAP 63, 2024. [3] A. Beckers et al., IEEE TED 67, 2020. [4] T. Mizutani et al., SNW 2021. **[Acknowledgements]** This work is based on a project, JPNP16007, commissioned by the New Energy and Industrial Technology Development Organization (NEDO), Japan and is also supported by JST SPRING, Japan, Grant Number JPMJSP2108.

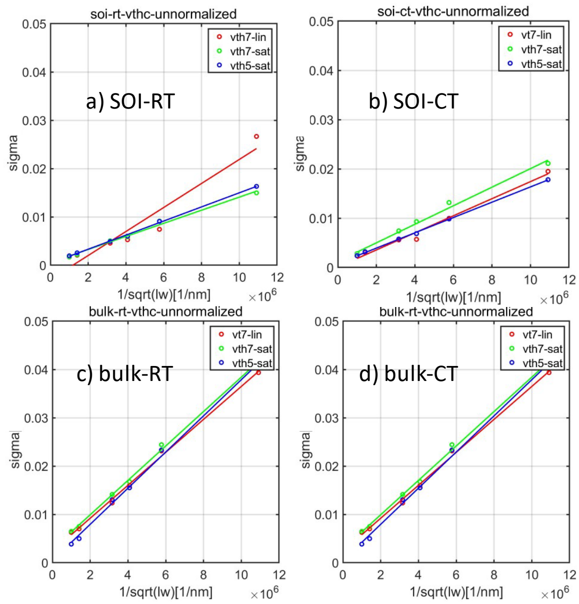

Fig.1. Vthc Pelgrom plots.

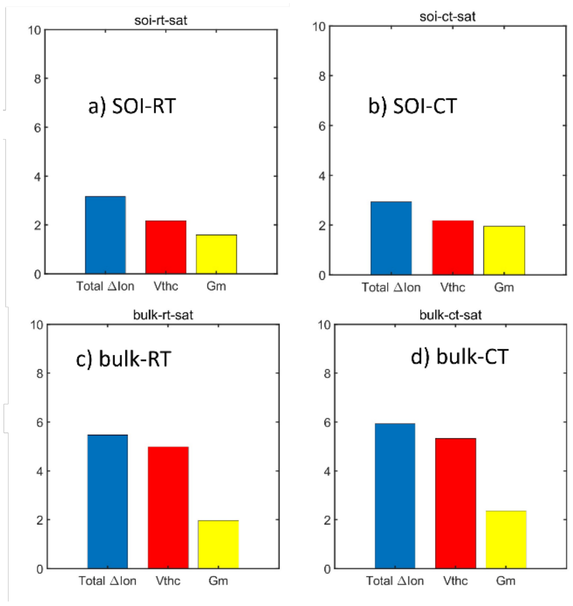

Fig.2. CT variability decomposition results for bulk and FDSOI FETs in saturation region.