強誘電体 AlScN 膜と酸化インジウムチャネルを用いた FeFET の試作

Fabrication of FeFET with ferroelectric AlScN film and In_2O_3 channel

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Introduction

Artificial intelligence (AI) and the Internet of Things (IoT) have become popular topics. To process and store large amounts of data, low-power consumption memory devices are required. Ferroelectric field-effect transistor (FeFET), featuring fast read/write speed, is one of the most promising candidates [1]. AlScN, a recently demonstrated III-N ferroelectric material, typically exhibits extremely high remnant polarization (P_r) along with low dielectric permittivity [2, 3]. Besides, In_2O_3 has drawn attention for thin film transistors (TFT) owing to its high mobility and wide bandgap [4]. Both AlScN and In_2O_3 can be processed below 400°C, and are compatible with the back-end-of-line (BEOL) process [3, 5]. In this work, we fabricated and characterized FeFETs with a ferroelectric AlScN layer and In_2O_3 channel.

Experimental methods

The FeFET device structure is shown in **Fig. 1**. A 20-nm-thick AlScN layer is deposited on top of the 10-nm-thick TiN gate electrode by sputtering. A 4-nm-thick Al_2O_3 layer is grown by atomic layer deposition (ALD), followed by a 3 nm In_2O_3 channel layer deposition by ALD. A TiN/W stack is deposited for Ohmic contact to the In_2O_3 layer.

Results and discussion

Fig. 2 delineates double sweep I_d-V_g characteristic curves of the fabricated FeFET. A clear counterclockwise hysteresis was obtained with a memory window of 1.1 V, indicating the FeFET operation. An on/off ratio of 10^9 was achieved, owing to the bandgap of In_2O_3. The voltage needed for the operation was 5 V. Note that a MOSFET with a 10-nm-thick Al_2O_3 layer without an AlScN layer, also shown in Fig. 2, exhibited a limited clockwise hysteresis, suggesting a decent interface property of Al_2O_3/In_2O_3.

Conclusion

A FeFET with $AlScN/Al_2O_3/In_2O_3$ structure is fabricated. Along with low operation voltage capabilities, a large memory window with a high on/off ratio was achieved. Compatibility with the CMOS process, this device holds great potential for development in next-generation memory technologies.

Acknowledge

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References

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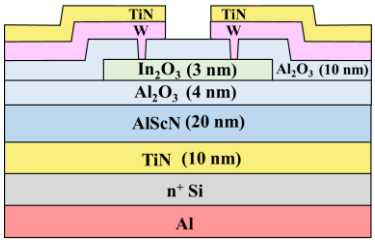

Fig. 1 Schematic diagram of the FeFET structure.

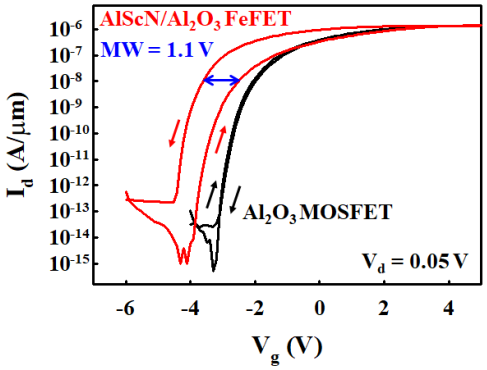

Fig. 2 I_d-V_g characteristic curves measured at V_d = 0.05 V.