異種チップレット三次元集積のためのダイレベル 3D-IC 作製技術

Die-Level 3D-IC Fabrication Technology for 3D Heterogeneous Chiplet Integration

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Abstract

This paper presents a cost-effective die-level TSV process for rapid prototyping of 3D-ICs from commercially available 2D-ICs called shuttle dies that are manufactured in foundry services. The 3D integration process employs advanced via-last TSV formation with temporary bonding/debonding and magnetron sputtering for high-aspect-ratio barrier/seed metal deposition without long-through ionized PVD. In this work, we successfully demonstrate heterogeneous 3D integration of a micro-LED array that is stacked on a 40-µm-thin 3D-IC with Cu-TSVs.

Introduction

The rapid prototyping of 3D-ICs is highly required for post-5G generation. More recently, 3D-ICs such as High-Bandwidth Memory (HBM) and 3D V-Cache have been widely used for supercomputers and generative AI applications. However, verification of new proof-of-concept with 3D-ICs is very limited. This is because there are very few chances that 3D-ICs will be readily available at low cost. This study presents a short turn-around time (TAT) 3D-IC fabrication scheme using via-last TSV and room-temperature Cu-Au bonding.

Method, Results and Discussion

As shown in Fig. 1, the fabrication process began with an enhanced temporary bonding technique to adhere a 2D-IC die to a glass wafer. An O_2-RIE process then precisely removed excess adhesive surrounding the die. This crucial step enhanced the bond strength and reduced warpage during subsequent CVD processes. Backside grinding and CMP were employed for thinning and planarization of 2D-ICs, reducing the die thickness to approximately 40 µm. A backside SiO_2 layer was then deposited with plasma-TEOS CVD.

The subsequent Cu-TSV fabrication utilized spray coating to ensure uniform photoresist thickness. Deep Si holes with an aspect ratio of within 4 were etched using the Bosch process, followed by liner (SiO_2) deposition via the plasma CVD technique. Next, a standard magnetron sputtering deposited the barrier/seed layer for the Si holes, followed by specialized bottom-up Cu electroplating to form Cu-TSVs. The void-free Cu-TSV is shown in Fig. 2 (a). Cu redistribution layers (RDL) are then formed. Finally, as shown in Fig. 2(b), 0.1-mm-cubed micro-LED are three-dimensionally stacked on the thin 3D-IC by using high-throughput pick-and-place and SAP (Semi-Additive Plating) [1] bonding to join the Cu-TSVs and Au electrodes of the micro-LEDs at room temperature.

Conclusion

This paper introduced a die-level via-last TSV fabrication process for 3D-ICs designed for rapid prototyping and cost-effectiveness. Utilizing readily available 2D-IC chips enhanced temporary bonding and controlled magnetron sputtering, enabling void-free TSV formation. Successful heterogeneous 3D integration was demonstrated with micro-LEDs and a thin 3D-IC fabricated at the die level from the shuttle 2D-IC die.

Ref.1) Y. Susumago & T. Fukushima, EDL, 44, 500 (2023).

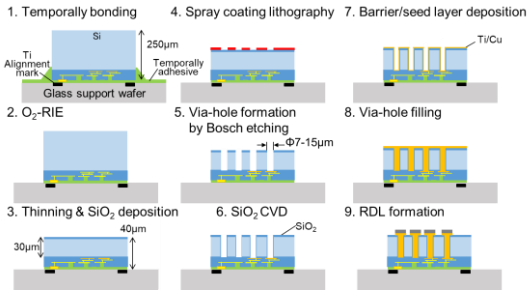

Figure 1. Via-last die-level TSV Process

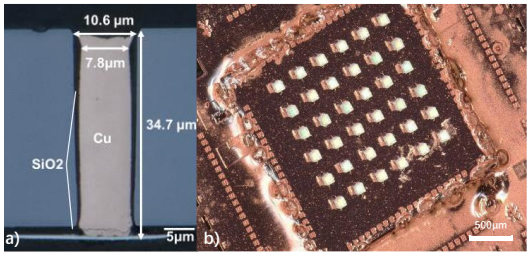

Figure 2. a) A cross-section of a Cu-TSV formed in a shuttle service 2D-IC at the die level with standard PVD (AR: 3.5); b) 36-Micro-LEDs stacking on 3D-IC chip by SAP bonding process

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