Study of interface trap density in Ge quantum devices

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Ge Hole spin qubit has shown potential for realizing high speed qubit operation [1] and large-scale qubit integration [2]. However, the strong spin-orbit coupling, which couples the spin degree of freedom to the electrical noise, poses challenges in maintaining high qubit fidelity while achieving the high-speed operation. Interface traps, a major source of electrical noise in the Ge quantum dots, therefore need to be studied to gain a comprehensive understanding of how to achieve long-term stable qubit operations.

In the previous report, people pointed out that higher atomic layer deposition (ALD) temperature results in a lower interface trap density [3]. Additionally, the application of oxygen plasma pretreatment [4] and pre-cleaning trimethyl-aluminum (TMA) pulse [5] are considered beneficial for oxidizing the Si cap and removing the GeOx, respectively. These treatments are potentially effective in reducing the interface trap density and, hence, improving the stability of the Ge quantum devices. Therefore, in this work, we applied these techniques and fabricated Hall bar devices (Fig. 1) with gate oxide film of Al_2O_3 deposited under different conditions on a Ge/SiGe heterostructure. We conduct a systematic discussion on the effect of ALD temperature (250°C and 150°C), oxygen plasma pretreatment, and TMA pre-cleaning on the quality of Al_2O_3 to identify the condition that enables the lowest interface trap density through capacitance-voltage measurements [6]. Furthermore, we investigate the dependence of hole mobility on carrier density, along with the percolation density, to demonstrate that a lower interface trap density gets the influence of surface tunneling effect suppressed. This study makes contributions to realizing a stable qubit environment in a Ge-based quantum dot system.

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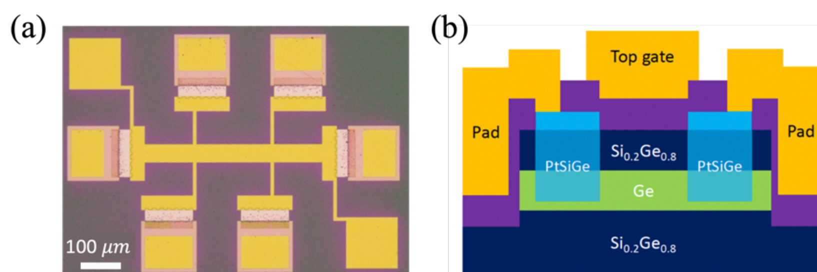

Fig. 1 A Ge Hall bar device. (a) optical microscope image. A lock-in measurement is performed to extract the longitudinal and transverse voltage differences. (b) Cross section of the Hall bar. Bonding pads are patterned on top of the $Si_{0.2}Ge_{0.8}$ virtual substrate to prevent the gate to Ohmic leakage.

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