

Potential-induced degradation of n-type front-emitter crystalline silicon photovoltaic modules with various encapsulants and cover materials

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[Introduction] Potential-induced degradation (PID) phenomenon can significantly impact the performance and lifetime of photovoltaic (PV) modules.¹⁾ PID is the performance degradation of PV modules caused by an electrical potential difference between an Al frame and the cells. In the case of n-type crystalline silicon (c-Si) PV modules, PID occurs under a negative bias through the accumulation of positive fixed charges in a front silicon nitride (SiN_x) layer, known as polarization-type PID (PID-p), and is characterized by simultaneous reductions in the short-circuit current density (J_{sc}) and the open-circuit voltage (V_{oc}).²⁾ For more diverse applications and higher material recyclability of PV modules, the PID of c-Si PV modules with various encapsulants and cover materials should be investigated. We have thus far investigated the PID of p-type c-Si PV modules with various module materials.³⁾ In this study, we performed the PID test of n-type c-Si PV modules using polycarbonate (PC) as cover material and polyvinyl butyral (PVB) as the encapsulation layer as well as conventional cover glass and ethylene-vinyl acetate copolymer (EVA).

[Methodology] Figure 1 shows the schematic structure of c-Si PV modules used in this study. We prepared n-type front-emitter c-Si solar cells from the commercial cells cleaved into $20 \times 20 \text{ mm}^2$. We used two types of encapsulant : EVA and PVB, and two types of cover material : glass and PC with a size of $45 \times 45 \text{ mm}^2$. The modules were formed by using a module laminator. The modules then received PID test by applying -1000 V to shorted module interconnector ribbons with respect to an Al plate placed on the cover glass of the modules in a chamber maintained at $85 \text{ }^\circ\text{C}$ with no humidity stress ($<2\% \text{RH}$) for up to 120 s. Current density–voltage (J – V) measurements were conducted in the dark and under 1-sun-illumination

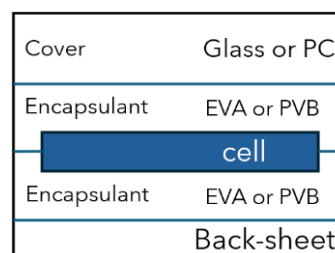


Figure 1. Schematic of the module structure.

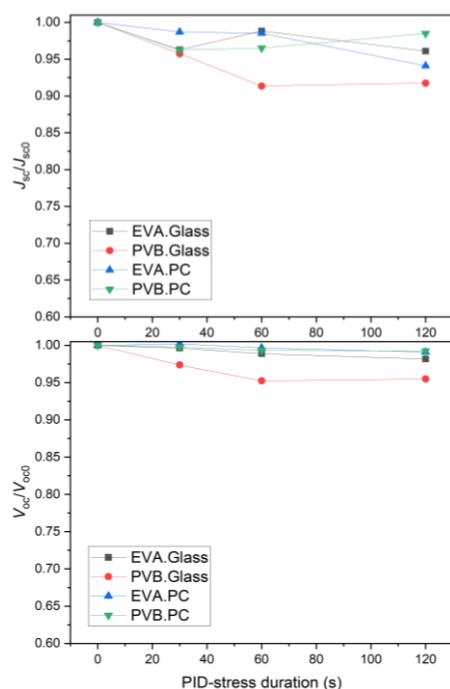


Figure 2. PID-stress duration dependence of J_{sc}/J_{sc0} and V_{oc}/V_{oc0} of 4 types of modules.

for the PV modules before and after the each PID tests.

[Results] Figure 2 shows the PID-stress duration dependence of J_{sc}/J_{sc0} and V_{oc}/V_{oc0} , where the subscript 0 indicates the initial value. The modules using EVA or PVB with cover glass shows decreases in V_{oc} and J_{sc} and their successive saturations. This is a typical behavior of the PID of n-type c-Si PV modules. In contrast, the modules with PC cover shows almost no decrease in V_{oc} . This clearly indicates that the use of PC as the cover of the PV modules can mitigate the PID-p of c-Si PV modules. Further experiments will be conducted to clarify to determine the duration for the saturation of the PID of the PV modules with PC cover.

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[References]

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