Component Prioritization Assessment in Gate-All-Around Nanosheet FETs using Design-Technology Co-Optimization (DTCO)

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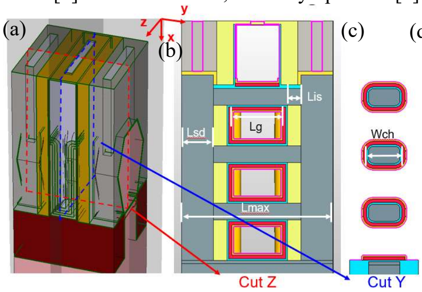
1. Introduction: Advanced CMOS device, notably Gate-All-Around (GAA) Nanosheet and Complementary FET (CFET), are crucial in navigating post-Moore era's challenges, such as quantum confinement and lithography limitations. Leading entities such as IMEC[1][2], TSMC[3], and Samsung[4][5] are advancing innovations in device characteristics and parasitic capacitance optimization across Middle-End-Of-Line (MEOL) and Back-End-Of-Line (BEOL). This study enhances a 5-track 3nm Nanosheet-based inverter cell and ring oscillator (RO) using Design-Technology Co-Optimization (DTCO), achieving performance and power enhancements of 7.7% and 10.2%, respectively. A novel component analysis by Multiple Regression Analysis (MRA) further identifies C_{MEOL} (MEOL capacitance) and device strategies as key factors for improving RO efficiency.

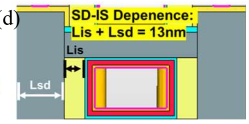
2. Simulation Flow: A DTCO approach is employed to optimize 3nm Nanosheet-based inverter and RO. **I)** TCAD models for NMOS and PMOS detail the profile, cross sections and default parameters in Fig. 1(a)-(c) and Table 1. Source/drain epi length (L_{sd}) and inner spacer length (L_{is}) show the trade-off (Fig. 1(d)). **II)** Compact BSIM-CMG models are extracted; RMS values are listed in Table 2. **III)** 5T inverter layout is designed using 3nm technology from [6]; cell interconnects are depicted in Fig. 3, along with extracted MEOL/BEOL capacitances and resistances in Fig. 4. **IV)** Hspice simulations of a 15-stage, 3-fanout RO are conducted (Fig. 5). **V)** A multivariate regression analysis (MRA) based on principal component analysis (PCA) evaluates the RO with 8 groups, focusing on SD-IS, contact resistance, and BEOL resistance dependencies (Fig. 6). Normalization, 5-fold cross verification, intercept term and lambda tuning are added to improve model accuracy and prevent overfitting.

3. Results and Discussion: Fig. 2 illustrates that increasing L_{is} leads to reduced drain saturation current (I_{dsat})and gate capacitance (C_{gg}) due to a longer effective gate length and thicker inner spacer, respectively. It is crucial to determine which factor—power consumption (I_{dsat}) or latency (C_{gg})—is more impactful. Fig. 3 displays low RMS, indicating high accuracy in compact model fitting. In Fig. 5, the L_{is} = 5nm case excels across all VDD levels, highlighting its speed and efficiency; this underscores the priority of minimizing parasitic capacitance over enhancing transistor performance (reducing I_{dsat}). Component analysis in Fig. 6 quantitively highlights MEOL capacitance and device performance, accounting for 51.7% and devices 40.9%, respectively. This underscores the need to prioritize MEOL capacitance reduction while also carefully improving transistor performance.

4. Conclusion: In this work, we investigated 3nm Nanosheet-based inverter cell and RO with DTCO flow. L_{is} = 5nm case improves performance by 7.7% and power by 10.2%. Component analysis through MRA reveals C_{MEOL} and device considerations are crucial for enhancing RO performance and efficiency.

References
[1] H. Mertens et al., VLSI Symp. 2023 [2] S. Mishra et al., VLSI Symp. 2024 [3] S. Liao et al., IEDM.2023 [4] S. K. Kim et al., VLSI Symp. 2023 [5] B. -S. Kim et al., VLSI Symp. 2024 [6] A. Veloso et al., EUROSOI-ULIS, 2019





Default transistor parameters [Unit: nm]		
Lg	Gate Length	15
Lis	Inner Spacer Length	4
Lsd	S/D Epi Length	9
Lmax	Max Length	45
Wch	Nanosheet Width	10

Fig. 1 (a) 3nm Nanosheet TCAD schematic. (b)(c) Z and Y cross-sections. (d) L_{sd} - L_{is} (SD-IS) dependency.

Table 1 Default transistor parameters in 3nm Nanosheet.

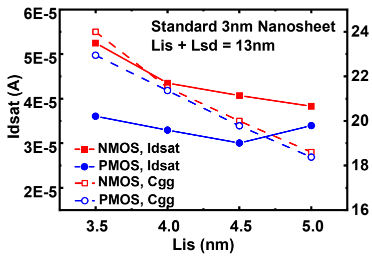


Fig. 2 Correlation of Drain Saturation Current (I_{dsat}) and Gate Capacitance (C_{gg}) with L_{is}.

Root mean square (RMS)		
PMOS	Id-Vg	1.94%
	Id-Vd	1.73%
	C-V	0.53%
NMOS	Id-Vg	1.13%
	Id-Vd	0.68%
	C-V	0.27%

Table 2 Root mean square in compact model extraction.

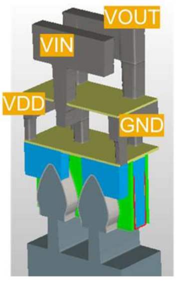


Fig. 3 Inverter cell schematic.

Critical Dimension [Unit: nm]	
Cell Height	105
Contact Gate Pitch	45[6]
Metal Pitch	21[6]
M0 Width	11
M1 Width	16

Table 3 Critical dimension in inverter cell.

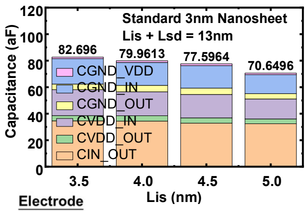


Fig. 4 MEOL& BEOL capacitance in inverter cell.

Electrode resistance [Unit: Ω]	
VIN	83.354
VOUT	39.823
VDD /GND	90.835

Table 4 MEOL &BEOL electrode resistance.

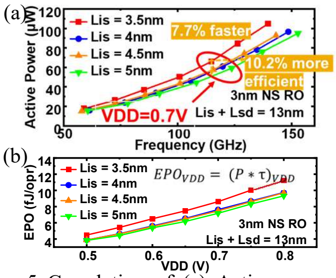


Fig. 5 Correlation of (a) Active power with frequency (b) Energy Per Operation (EPO) with VDD under different L_{is} in 15-stages ring oscillator (RO) simulation.

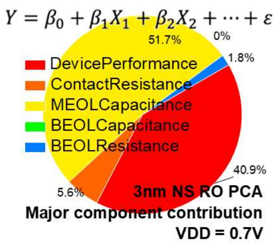


Fig. 6 Multivariate Regression Analysis (MRA) on RO based on Principal Component Analysis (PCA) with samples in 8 groups.