Design Technology Co-optimization (DTCO) for spacer Design in Gate-All_around Nanosheet FETs

[1]IIS, The Univ. of Tokyo, [2]d.lab The Univ, of Tokyo ○Yaoping Xiao[1], Xiaoran Mei[1], Takuya Saraya[1], Toshiro Hiramoto[1] and Masahara Kobayashi[1] **E-mail: yp-xiao@nano.iis.u-tokyo.ac.jp**

Introduction: With continuous feature-size scaling, Gate-all-around Nanosheet (GAANS) has been considered as a candidate for 3nm technology node and beyond because of its excellent gate controllability [1]. However, the trade-off between the lengths of different sections along the channel direction of the device such as gate, spacer and contact in Front-of-Line (FEOL) and Middle-of-Line (MOL) can have a significant impact on the performance [2-3]. Besides, resistance and capacitance (RC) of Back-End-of-Line (BEOL) interconnects also play significant roles in impacting circuit's power-performance-area (PPA) [4]. In this work, following the principles of DTCO, we discuss the impact of deveice geometry of a GAA NS FET, as well as RC of interconnects on the power-performance if a ring-oscillator circuit.

Simulation Methodology: We developed simulation-based DTCO framework as shown in **Fig.1.** First, we set a design rule and process assumption for 3nm technology and beyond, and simulated DC characteristics of GAA NS FET using TCAD. These characteristics are then fitted to extract SPICE model. Simultaneously, an inverter based on GAA NS FET was designed, and 3D process emulation model was built including interconnects. Next, RC of the interconnects was extracted by the emulation tool. Finally, the SPICE netlist was combined with the extracted RC to evaluate the power-performance of a ring oscillator as AC characteristics. We did the same procedure for different device geometry.

Results and discussions:

(1) Device characteristics: The simulated I_d-V_g and I_d-V_d curves as well as spice model fitting results are shown in **Fig.2.** Threshold Voltage(V_{th}), subthreshold swing(SS), on-state current and Drain-Induced Barrier Lowering(DIBL) for the nominal NFET and PFET are as follows: V_{th}:0.166V for NFET and -0.161V for PFET;SS:84.055mV/dec for NFET and 82.809mV/dec for PFET; On-state current:3×10^{-5}A for NFET, -5×10^{-5}A for PFET; DIBL:30.107mV/V for NFET and 31.077mV/V for PFET. The devices behave well with suppressed Low Voltage Threshold (LVT) short channel effect. The Root Mean Square Deviation (RMSD) fitting errors of the I_d-V_g and I_d-V_d for NFET are 3.6% and 2.9% respectively, for the PFET are 2.0% and 2.8% respectively. The fitting accuracy is acceptable in this work.

(2) Ring Oscillator circuit performance: Fig.3. shows the impact of the device geometry among the low-k inner spacer thickness and the source and drain contact width, gate length and high-k gate dielectric thickness on the power-performance of the RO circuit. As inner spacer thickness increases, the RO has high performance at the same power or has the same performance at the lower power. The low-k inner spacer is a key design element for high performance and lower power circuit in GAA NS FET technology, particularly reducing parasitic capacitance.

Summary: Based on the DTCO approach, we simulated the impact of the device geometry of the GAA NS FET on the power-performance of the RO circuits. The results highlight that with the continuous scaling of technology nodes, parasitic parameters have sighifhcant impact on circuit power-performance.

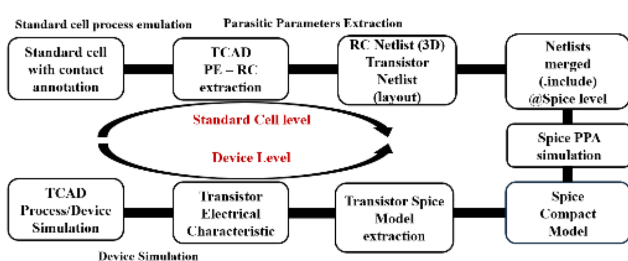

Figure 1 DTCO process

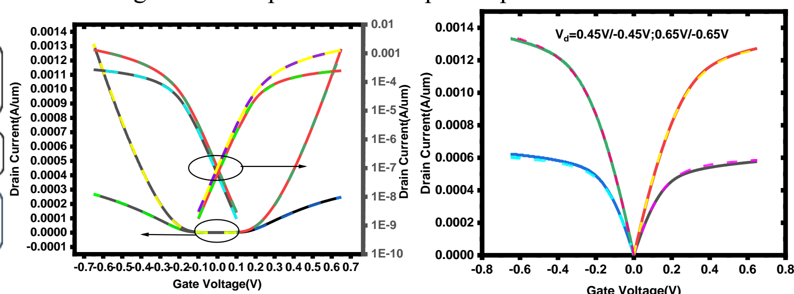

Figure 2(a) IdVg curve of Device(b)Idvd curve of Device

Reference:

[1] N.Loubet et al. VLSI 2017.**[2]** D.Ryu et al. TED 2020. **[3]** Velsos A et al. EUROSOI-ULIS. 2019. **[4]** Huang,Victor,et al TED 2594-2599.20

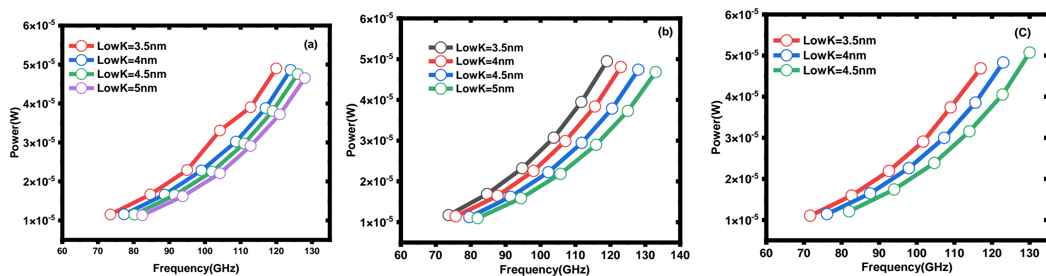

Figure 3(a)Lowk Inner spacer with S/D contact(b)Inner spacer with gate length(c)Inner with high-k gate dielectric thickness

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