Comprehensive Study on the Silicon-Nanosheet Thickness Dependence On the Device Performance of Gate-All-Around NFETs

[1]IIS, The Univ. of Tokyo, [2]d.lab The Univ, of Tokyo ○Yaoping Xiao[1], Xiaoran Mei[1], Takuya Saraya[1], Toshiro Hiramoto[1] and Masaharu Kobayashi[1,2]
E-mail: yp-xiao@nano.iis.u-tokyo.ac.jp

Introduction: With the continuous scaling of transistors and the reduction in gate length (L_g), short-channel effects (SCE) become increasingly severe. Compared to the traditional planer devices and FinFETs, Gate-All-Around Nanosheet (GAA NS) FETs exhibit superior gate control capabilities [1-2]. It is generally necessary to reduce L_g of devices to scale down Contacted Poly Pitch (CPP) for shrinking standard cell size. Besides, NS needs to be thinned down to suppress SCE. As NS thickness becomes thin, the quantum confinement becomes pronounced. In past research, many efforts have been made to understand the impact of NS thickness on the performance of NS FETs [3-4]. To comprehend prior works and explore the thickness scaling limit, we systematically study the influence of thickness scaling on the performance of GAA NS FETs by incorporating low-field mobility models and high-field quasi-ballistic transport as well as band structure calculated with quantim confinment [5].

Simulation Methodology: The simulation procedure for GAA NS NFETs is shown on **Fig.1.** First, band structure was calculated by k.p Hamiltonian method. At given surface orientation and temperature, 2D Schrödinger equation was solved for the NS cross section, which was repeated along the channel direction. Then, 1D Boltzmann transport equation (BTE) was solved under the given boundary conditions, coupled with inter- and intra- subband phonon scattering, Coulomb scattering, and surface roughness scattering. Finally, the charge distribution under quantum confinement was coupled into the 3D Poisson equation for updating the electrostatic potential. This procedure was repeated until the charge distribution and electrostatics potential were converged in self-consistent Poisson-Schrodinger solver.

Results and Discussion: Fig.2(a) shows on current decreases with sheet thickness scaling down, but **Fig.2(b)** shows normalized on current reaches its optimum value when thickness equals 3nm. **Fig.2(c)** shows subthreshold swing (SS) versus sheet thickness. SS is improved as the sheet thickness decreases; however, when the sheet thickness becomes less than 3 nm, SS is deteriorated due to quantum confinement (QC). **Fig.2(d)** shows that the injection velocity of electrons increases as the sheet thickness decreases, and this increase becomes more pronounced with higher inversion layer charge density. This is due to the quantum confinement effect, which causes electrons to populate the 2-fold valleys with smaller effective mass. **Fig.2(e)** shows that the threshold voltage (V_{th}) increases as the sheet thickness decreases. This is because the QC effect raises the energy subband levels and requires higher gate voltage for electron population.

Summary: We comprehensively studied the impact of sheet thickness scaling on the performance of NS NFETs incorporating relevant physics. We observed that continuous reduction in sheet thickness does not necessarily lead to gaining device performance; instead, there exists an optimal thickness at which the device performance is maximized. This work provides an insight into NSFET scaling.

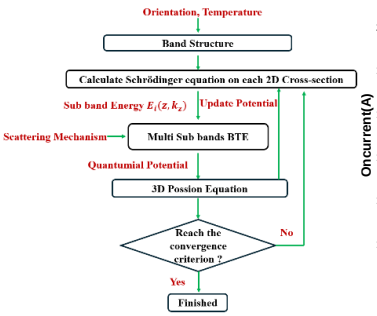

Figure 1 Flow chart used in this work

Reference:[1]Bae.Geumjond.et al IEDM 2018
[2] Loubet.N et al VLSI 2017
[3]N. Neophytou.et al TED 2008
[4] C. Medina-Bailon etal EDL 2019
[5]Sentaurus Device QTX user Guide Synopsys Mountain View. CA USA Dec.2023

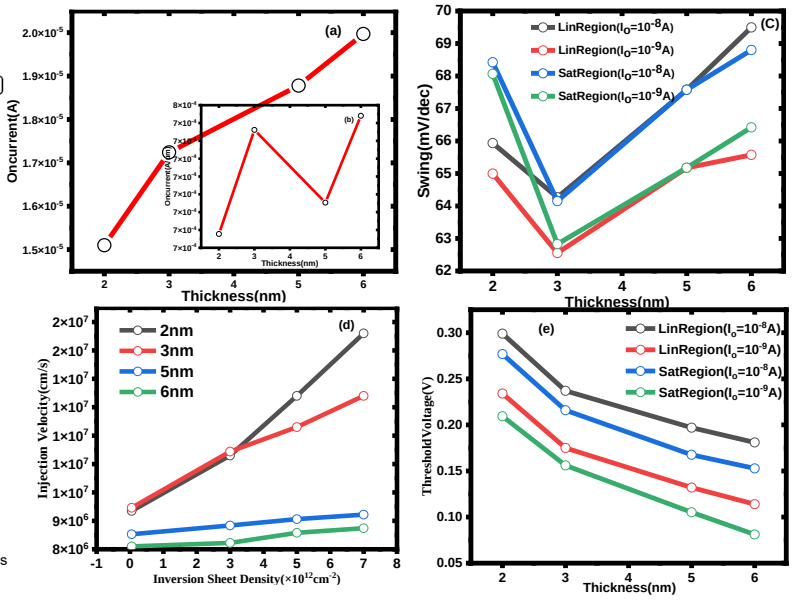

Figure 2 Characteristics of NSFET different thickness