6-5 AN IMPROVEMENT ON STRUCTURE OF CHARGE-COUPLED DEVICES

Tadayoshi MIFUNE, Shigeyuki OCHI, and Yasuo KANO

SONY Corporation Research Center

174 Fujitsukacho, Hodogaya-ku, Yokohama, JAPAN 240

We report an improved structure of a charge-coupled device by placing high resistive material between transfer gate electrodes on gate oxide.

In a CCD with gate electrodes of single layer, the electrode separation is several micrometers, and a potential barrier is inclined to arise under SiO_2 of these inter-electrode gaps. For the complete transfer of charge in a CCD, such a potential barrier must be reduced. To satisfy this requirement, we have to place the electrodes sufficiently close. Where a transferring charge is a hole, an existence of interface states makes the potential barrier larger, and depletion layer width at the surface is reduced as compared with that of the interior of the Si substrate. In Fig. 1, a reduction of a surface depletion layer vs V_{th} is shown by a simple calculation. This condition requires closely spaced electrodes and, accordingly, more difficult photolithographic technique. Actually we have hardly got a CCD in action on a condition of 2.5 v threshold voltage and 3 μm inter-electrode gap width on a 10Ω-cm N-type substrate. However, when the surface of SiO_2 is contaminated (for instance, a hydrated surface of phosphorous silicate glass), the dirt adhered to the surface polarizes and forms a temporary electrode which eliminates the potential barrier, then the CCD gets in operation. But this polarized layer has a large time constant and influences undesirably on the charge behavior.

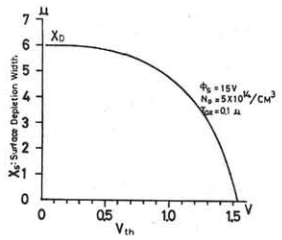

Fig. 1
Reduction of Depletion layer at Surface vs V_{th}

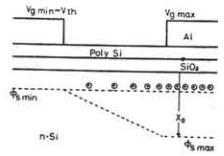

Fig. 2
Cross Section View

Metallization of a single layer is a simple method for the CCD fabrication unless before mentioned situation at a gap makes any trouble.

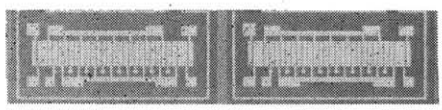

Fig. 3
3 Phase 8 Bit CCD

We introduce a high resistive material on SiO_2 of inter-electrode gap, whose potential is controlled by the difference of the adjacent electrodes, and maintains a certain potential which is generally

above V_{th}. Fig. 2 shows a cross section view of this CCD with polycrystalline silicon as a high resistive material. The device has been fabricated on a nominal 10Ω-cm N-type substrate with (100) orientation. A gate oxide film of 0.1 μm thick was grown at 1100°C in dry O_2, then polycrystalline silicon was deposited chemically at 670°C followed by evaporation directly over it.

Thus we constructed a 3 phase 8 bit CCD with a gate area of 250 x 50 μm^2 as shown in Fig. 3.

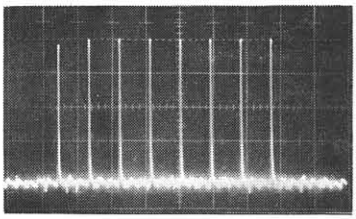

Fig. 4 Characteristic
100μs/div
0.1 V/div

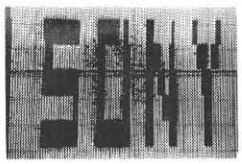

Fig. 5
Single Line Scanner

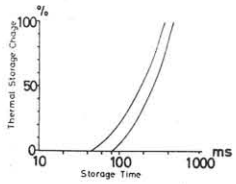

Fig. 6
Thermal Storage Time

A characteristic of the shift register at 11.1 kHz is shown in Fig. 4. Fig. 5 shows our application of this device to a single line scanner as an image sensor. Fig. 6 shows its thermal charge generation time.

Stable operation of a CCD with inter-electrode gap of 5μm and a V_{th} of 4 v was achieved.

We also achieved in reducing the severe requirements on photolithographic technology and the surface condition.

Acknowledgement

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References

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