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B6-3 CONTINUOUSLY VARIABLE THRESHOLD VOLTAGE DEVICES

by

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A new MOS device, of which threshold voltage is continuously varying a horizontal direction under the gate electrode, has been proposed and developed. It is called the continuously variable threshold voltage device (CVTD). This paper will describe the principles and the structures of the CVTD and its applications such as MOS-FETs with remote-cutoff characteristics, voltage variable MOS-type varactors, high speed self-scanning devices, high speed clockless A/D converters and their experimental results to some extent.

Since the threshold voltage of MOS-FET depends on the amount of charges in the insulators or substrates under the gate electrode, two different methods have been proposed and demonstrated in order to realize the CVTDs. They are to use the followings;

1) the continuous change of the threshold voltage responsible for the locational dependence of the fixed interface charges injected into the double-insulator gate structure as well as MNOS[1),2)] and MAOS[3),4)] memory devices. (Injection type CVTD: INJ-CVTD)
2) the continuous change of the threshold voltage responsible for the locational dependence of the fixed bulk impurity charges implanted into the thin surface layer of the substrate by use of a new technology named the Lateral Impurity Microprofiling (LIM) by Ion Implantation. (Lateral Impurity Microprofiling type CVTD: LIM-CVTD)

Fig. 1 a) and b) show the cross sectional views of the INJ-CVTD and LIM-CVTD. Fig. 1 c) shows the shape of the induced channel under the gate electrode of the CVTD, of which threshold voltage varies linearly along the direction perpendicular to the source and drain direction.
Fig. 2 shows how the threshold voltages change under the gate electrode for both the INJ- and LIM-CVTD. The basic electrical characteristics measured on a INJ-CVTD is shown in Fig. 3. These experimental results indicate that the threshold voltage between Z_1 and Z_4 in Fig. 1 c) varies from 3.0 to 19.5 volts. As a result, the induced channel extends from Z_1 towards Z_4 depending on the applied gate voltage.

Replacing a source electrode by a number of divided small source electrodes as shown in Fig. 4, one can use the CVTD as the new switching device. Fig. 5 shows a high speed clockless 5 bits A/D converter by use of CVTD concept.

References

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3) P. Balk and F. Stephny: J. Electrochem. Soc., 118, 1634, (1971).
4) S. Sato, T. Yamaguchi and T. Aoki: 1972 IEEE Int. Solid State Circuit Conf., Digest of Technical Papers, p.88 (1972). S. Sato and T. Yamaguchi: to be published in Solid State Electronics, 1974.

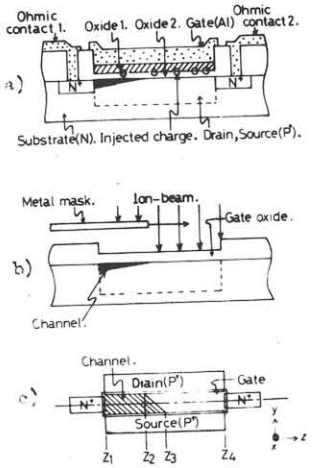
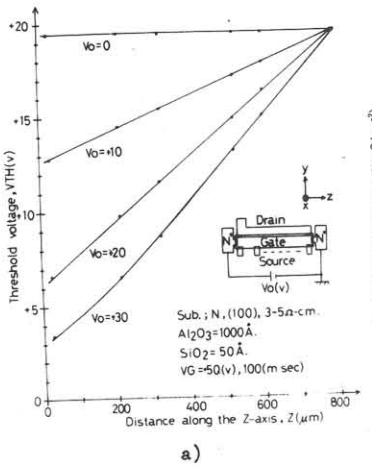


Fig. 1: The device structure of the CVTD
a) A crossectional view of the INJ-CVTD
b) A crossectional view of the LIM-CVTD
c) A surface channel shape of the CVTD



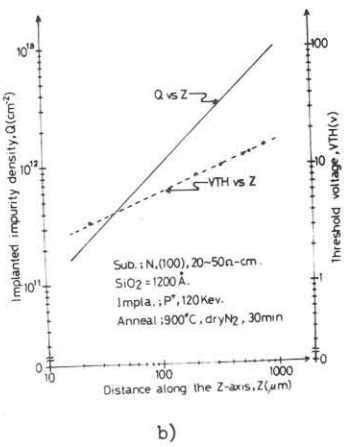
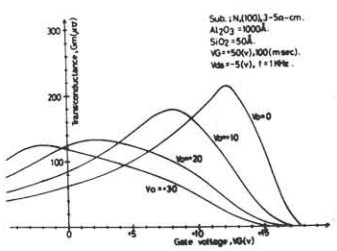
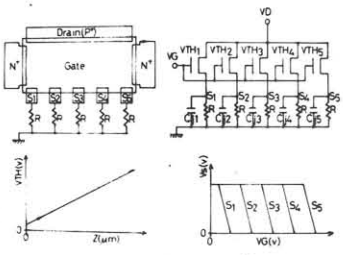
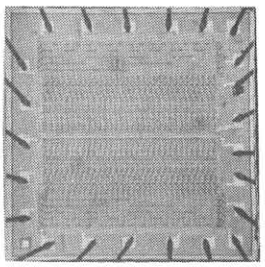


Fig. 2: The locational dependence of threshold voltages and surface impurity density in INJ-CVTD and LIM-CVTD
a) INJ-CVTD
b) LIM-CVTD







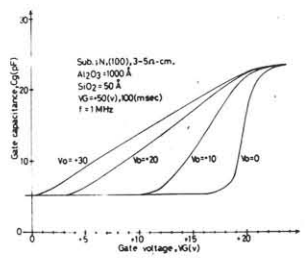


Fig. 4: A self scanning device by use of the principle of CVTD
a) The device structure
b) An equivalent circuit model of self scanning device

Fig. 3: A fundamental characteristics of INJ-CVTD
a) A transconductance: g_m VS gate voltage: V_G
b) A gate capacitance: C_g VS gate voltage: V_G

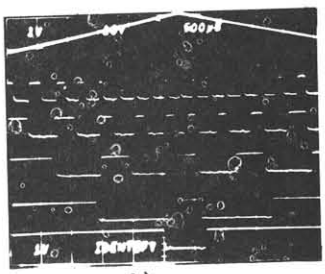


Fig. 5: The clockless A/S converter
a) A photograph of 5 Bits clockless A/D converter
b) A photograph of the in-put and out-put signal for 5 bits clockless A/D converter