B-2-3 DESIGN AND EVALUATION OF 64K-BIT MAGNETIC BUBBLE MEMORY CHIP

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It is urgently desired to realize mass capacity magnetic bubble memory chips when their practical level applications are considered. Up to present, 16k-bit chips have been developed and satisfactory operations are confirmed[1),2)]. Basing on these results, we have fabricated major-minor organized 64k-bit chips. All the device functions have been examined and found fully operational at a rotating field frequency of 100kHz with a reasonable bias field margin. In this paper, we describe the design of 64k-bit chips and report the results of the operation.

In Fig.1, a photogragh of the 64k-bit chip is shown. The basic chip design has been modified only insofar as a bit size and detector circuits are concerned; the functions of replicate/annhilate, generation and transfer remain as described for the 16k-bit chip[2)]. There are 128 minor loops. Each minor loop contains 513 bits with a bit size of 20μm x 20 μm. The detailed dimensions of propagation circuits are listed in Table 1. Those optimum values g, w, and s are determined by examining propagation performance of various circuits with different pattern element sizes. Two fish-bone detectors are placed adjacently in the chevron stretcher. These are so arranged as to do noise-cancelling in an efficient way[3)].

The LPE film is of $(YSm)_3(FeGa)_5O_{12}$ with a demagnetized strip width of 4.7μm.

The chip tested was fabricated with no defects. Namely, all minor loops operated normally. The overall operating bias field margin diagram is shown in Fig. 2. The measurements were carried out in a memory module. Typically a margin of 10% was observed. The detailed results on all device functions will be presented.

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REFERENCES

1) P. I. Bonyhard et al., IEEE Trans. Mag., MAG-9, 433 (1973)

2) M. Hiroshima et al., 1974 IECE Conf. No.267

3) P. C. Michaelis et al.,IEEE Trans. Mag. MAG-11, 21 (1975)

Table]. T-Bar circuit parameters

Period λ	20 μm
T-Bar gap g	].3 μm
Bar width w	2.6 μm
Spacing* s	].] μm
T-Bar thickness	4000 Å

* Distance between the circuit and the LPE film

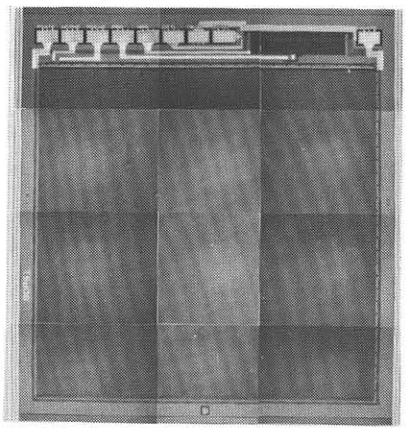

Fig.]. The 64k-bit memory chip. The chip size is 6.5mm x 6.0mm.

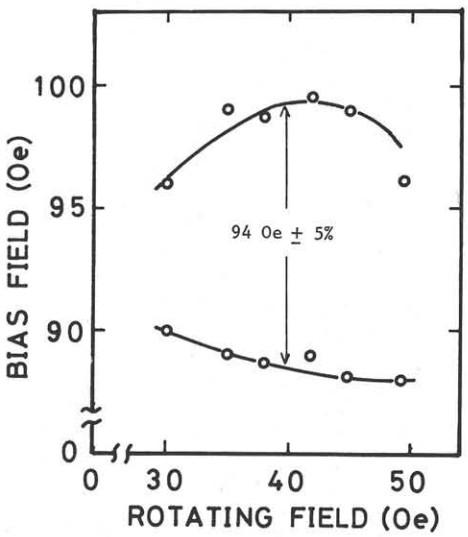

Fig.2 Operating margins.