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D. R. Breuer and A. S. Templin
TRW Systems, One Space Park, R6/2529, Redondo Beach, CA 90278, (213) 535-1017

A-2-5 # High Precision, High Speed Analog/Digital LSI Techniques

Introduction

Techniques have been developed to achieve analog-digital bipolar LSI functions which provide better than 0.1% analog accuracies at speeds of 50-100 MHz. This performance level is achieved by directing attention at the process, device, and circuit level. High speed requires small junction areas for low capacitance, in contradiction to the large junctions normally necessary for device matching. Proper choice of circuit techniques minimizes this conflict, coupled with a judicious choice of device geometries. A monolithic thin film cermet resistor technology and an ion implanted bipolar transistor form the processing base for achieving the stated performance levels at LSI complexity levels (2500-3500 devices per die).

Process/Device Description

The integrated circuit devices are shown in Figure 1. Doping is controlled by ion implanting a 0.5 μm boron base and a 0.3 μm arsenic emitter. Ion implantation provides the control necessary to achieve transistor beta matching of 1% and V_{BE} matching of 0.1 mv. The use of arsenic offers additional diffusion control and an optimum doping profile for high f_T values, low r_b', and excellent matching. A recut emitter process uses a 4x6 μm emitter contact, with 3 μm mask-to-mask spacing. Positive photoresist, contact printing, and hard chrome masks assure tight dimensional control. This results in matched transistors with f_T = 2 GHz at V_{CB} = 0 volts, and C_{CB} = 0.3 pf at V_{CB} = 0 volts.

High accuracy, low parasitic cermet (Cr·SiO) thin film resistors are evaporated. An intermediate film of molybdenum is used for precisely patterning the resistor and is removed after cermet etching. This results in batch fabricated resistors with better than .05% matching and .02pf/mil^2 parasitic capacitance to substrate. Individual resistors can be laser annealed to trim to better than .01% for even higher accuracies. The use of cermet allows tailoring of sheet resistance to provide a constant power-delay product over a wide frequency range, leaving the semiconductor processing undisturbed. Sheet resistances can be varied from 100 to 1000 ohms per square.

A two-level aluminum interconnect system gives low parasitic capacitance and the layout flexibility needed to optimize the design for minimum interconnect capacitance and optimum thermal characteristics.

Circuit Description

Analog-to-digital converters have been designed and fabricated with these techniques with the following characteristics: 8 bit ± 1/4 LSB, 10 Ms., 10 bit ± 1/4 LSB, 5 Ms., and 12 bit ± 1/4 LSB, 2 Ms. The 8 bit and 10 bit diffusions have been obtained with good yield by simple batch fabrication techniques. The 12 bit design requires laser resistor trimming. Figure 2 shows the block diagram of these single bit feedback, successive approximation converters. A strobed comparator[1] is used with a small signal tracking gain of four and a positive feedback hold mode which synthesizes infinite gain for creating a ditital decision. In the 10 bit design, this provides a set-up time of 1 nsec. and a

propagation delay of 4 nsec., resolving a LSB of 2.0 mv. A D/A uses ten equally weighted current sources switched into a 200 ohm R-2R ladder network. Each current source delivers 7.7 ma. and results in a D/A settling time of 10 nsec. The low parasitic capacitance of the ladder resistors play an important factor in this high speed response. The precision current source transistors and emitter resistors have oversized geometries to minimize errors. This is convenient since these devices are not switched. The D/A latch adds another 1 nsec. delay resulting in a total loop delay of 16 nsec. The entire conversion cycle requires 12 time bins and takes less than 200 nsec. Figure 3 shows a reconstructed ramp, visually demonstrating the linearity of this converter. There are no missing codes at the specified sample rate.

Device accuracy measurements have not been taken, however, the major sources of error include: resistor ratios, V_{BE} matching, beta matching, collector output impedance, and thermal differentials. The overall A/D linearity has been measured to less than 0.4 LSB, RSS over the temperature range of -30°C to 65°C at a sample rate of 5 Ms./sec.

Low level differential logic[2] is used throughout to achieve optimum power-delay product. This logic form provides from 4 to 6 times lower power than standard ECL techniques. The 10 bit converter described consequently draws 2.7 watts of power.

Conclusions

It is evident that with careful engineering techniques at a processing, device and circuit design level, accuracies of better than 0.1% can be achieved at clock rates of 60 Ms./sec.

Acknowledgements

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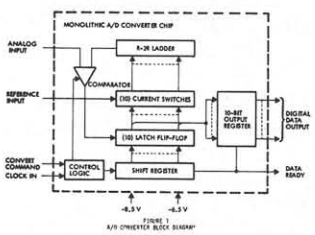

FIGURE 1
A/D CONVERTER BLOCK DIAGRAM

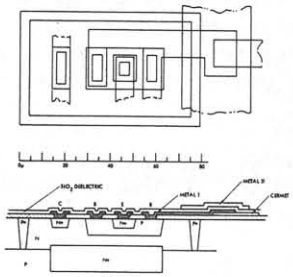

FIGURE 2
INTEGRATED CIRCUIT DEVICES

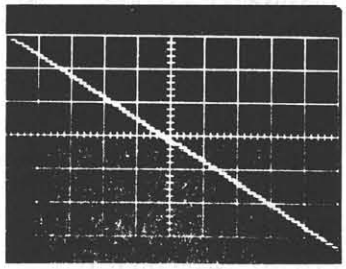

FIGURE 3
RECONSTRUCTED RAMP WAVE FORM, EXPANDED SCALE, SHOWING 3/4 POINT AT 60 MHz CLOCK

[1]Breuer, D. R. "High Speed A/D Converter Monolithic Techniques", ISSCC Digest of Technical Papers, p. 146-147, February 1972.

[2]Breuer, D. R., "Applications of Low Level Differential Logic", ISSCC Digest of Technical Papers, p. 126-127, February 1975.