A—1—3 A Subnanosecond Masterslice LSI using Dielectric Isolation and Three Layer Metallization Technologies

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A high speed bipolar masterslice LSI has been realized using dielectric isolation and three layer metallization technologies.

Dielectric isolation technology is an effective process for reducing parasitic capacitance and increasing packing density of integrated-circuit. Figure 1 illustrates a cross section of the NPN transistor, which is isolated by oxide in N-type epitaxial layers of 2.1μ thickness. This process offers an easy control of base width and consequently high f_T transistor in comparison with P-type epitaxial Isoplanar process. Table 1 shows the characteristics of the transistor with 4 × 12.5 μ^2 emitter, in comparison with the conventional ECL 10K process transistor.

When conventional two layer metallization is used, a greater part of chip is occupied by wiring area, especially by power supply lines. While, three layer metallization technology is effective to reduce wiring area and chip size by assigning power supply lines on the third level metal. Planar Metallization with Polymer (PMP) technique[1,2] has been employed for three layer metallization because of the following reasons. PMP structure has the advantages of good planarity and possibility of a thicker polyimide film compared with conventional structure with SiO_2. It results in easy formation of fine pattern on any metal layer, reduction of capacitance between layers and high yield.

Using these technologies, the masterslice LSI has been fabricated. Figure 2 illustrates an internal gate, realized by the CML circuit with a logic swing of 400 mV and with emitter follower together with extensive use of collector-dotting and emitter-dotting. Because of low parasitic capacitances, average propagation delay of 0.7 ns can be achieved for this basic internal gate (fan-in of 2, fan-out of 1) with only 0.3 mA of switching current, which results in reducing power dissipation. The internal gates are connected with LSI pins via output level converters to obtain a compatibility with standard ECL.

The LSI contains 100 blocks of 4 internal gate cells, 60 output gate cells, 60 output emitter follower transistors and 50 reference circuits. A block occupies 0.22 mm^2, containing wiring area, with 32 transistors, 2 diodes and 29 resistors. For example, an internal gate with fan-in of 3 can be composed by one cell. Figure 3 is a microphotograph of this LSI. The chip size is 5.7mm × 5.7mm and 63.8% of whole area is occupied by internal gate cells. The minimum metal line width and space between metal lines are 6μ and 4μ, respectively. The minimum

through-hole sizes are; 6μ × 6μ between the first and the second layers, 14μ × 15μ between the second and the third. Table 2 shows the characteristic features of the ALU chip by this masterslice LSI.

References

1. K. Sato et al.: IEEE Trans. Parts, Hybrids, Packag., Vol. PHP-9, p.176, September,1973.
2. A. Sakai et al.: National Conv. Rec. of IECE Jap., No.259, 1977.

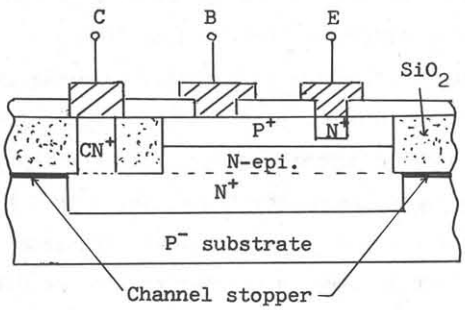

Figure 1 - A cross section of the NPN transistor

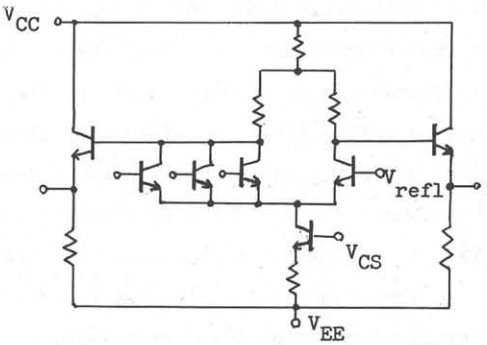

Figure 2 - An internal gate

Items	Oxide isolated transistor	Conventional transistor	Note
Base-emitter junction capacitance	0.16 pF	0.223 pF	V_J=-0.o V
Base-collector junction capacitance	0.25 pF	0.43 pF	
Collector-substrate junction capacitance	0.63 pF	1.65 pF	
Cut off frequency: f_T	1.8 GHz	1.5 GHz	
Current gain: h_{FE}	70		
Collector area	0.46	1	
Base area	0.83	1	

Table 1 - Characteristics of the NPN transistor which is isolated by oxide in N-type epitaxial layers in comparison with the conventional ECL 10K process transistor

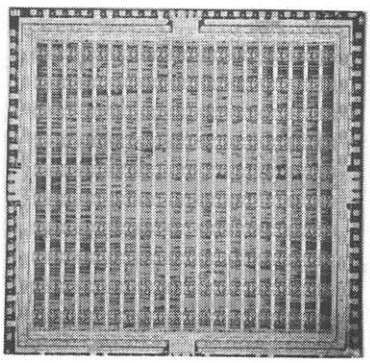

Figure 3 - A microphotograph of the masterslice LSI.

No. of circuits	394 internal gate cells 50 output gate cells
Power supplies	V_{CC}=GND, V_{EE}=-3.2 V
Chip size	5.7 mm × 5.7 mm
power dissipation	2.59 mW (50 ohm termination)
Delay time	1.48 ns per circuit 0.82 ns per function

Table 2 - Characteristic features of the ALU chip