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A DSA-type Non-Volatile Memory Transistor with Self-Aligned Gates

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Introduction Two main types of n-channel non-volatile memory devices with stacked-gate structure have so far been developed and successfully applied to (1) EPROMs[1]-erasable and programable read only memories, and (2) EEPROMs[2,3]-electrically erasable PROMs. However, each of these devices is conceivable to have the following two main disadvantages and has room for further improvement. For the E-type devices, they are ; (a) the high surface impurity concentration which makes so called channel electron injection[4,5] efficient causes the threshold voltage shift and makes the conductance of memory transistor poor, and (b) the erasure is slow because the control-gate of second poly.Si absorbs the U.V light. On the other hand, for the EE-type devices ; (a)' high integration is difficult because the cell requires a switching transistor compared to 1Tr/bit organization of E-type devices, and (b)' in erasure operation, both polarities of applied voltages are necessary. The memory transistor proposed here is applicable for both types of devices (E or EE), and is eliminated of all above mentioned disadvantages.

Preparation of Samples Fig. 1 outlines an example of main processing steps of the proposed memory transistor. In this figure, (A) starting with π-type Si substrate, thick field SiO_2 and channel stopper P-region self-aligned with it are formed using LOCOS technique. After that ~800Å first gate SiO_2 and ~1000Å first poly.Si are successively grown. (B) Control and floating gates are patterned self-aligned with each other after the growth of ~1000Å second gate SiO_2 and 0.5 μ second poly.Si. (C) The P^+-region self-aligned with both gates is formed by the ion implantation of boron. (D) By phosphorus diffusion, source and drain N^+-regions are formed which are self-aligned with both gates. Drain N^+-region is also diffusion-self-aligned (DSA) with the P^+-region. (E) Following the well known steps, the device is completed.

Experimental Results This memory transistor with new structure can be written by channel electron injection and erased by optical or electrical means. Writing and erasure characteristics are measured as threshold voltage shifts of the memory transistor (V_{TM}). V_{TMO} is the original V_{TM} when the floating gate is not charged.

Fig.2 and Fig.3 show writing characteristics with V_W and V_{CG} as parameters respectively for the memory transistor on 100Ω-cm substrate. Write pulse V_W is applied to the drain through a series resistor of 1KΩ with the control gate voltage V_{CG} positive.

Fig.4 shows erasure characteristics for stacked-gate memory transistors exposed to short-wave ultraviolet (λ=2536Å) of 8W mercury lamp. Comparing with conventional devices, this new device has a excellent characteristic because U.V. light illuminates directly the edge of the floating gate which is not covered by the control gate.

Electrical erasure can be performed by surface avalanche hole injection from the source junction. In this DSA structure, P-type impurity concentration of the substrate is possible to be low, so that the surface breakdown voltage at the source junction is not limited by the impurity concentration and it rises with increase of the floating gate potential. Hole injection stops when the surface breakdown voltage becomes equal to the erasure voltage V_E applied to the source. By this reason, saturation level of V_{TM} shift is determined by V_E only when V_{CG} grounded. However, a substrate with such low impurity concentration as it makes the surface except for the P^+-region normally inverted, is not applicable for electrical erasure because the breakdown is not controled by the floating gate potential but by the impurity concentration of the P^+-region. For the EE-type device, we used a substrate of 13Ω-cm resistivity, in which the surface is weak enhancement. The experimental results for electrical erasure are shown in Fig.5. Erasure pulse V_E is applied to

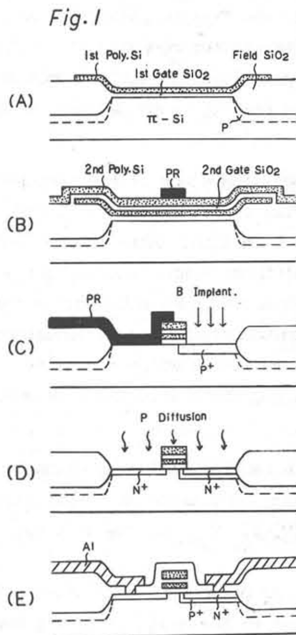
the source through a series resistor of 1KΩ with the drain terminal open and V_{CG} grounded.

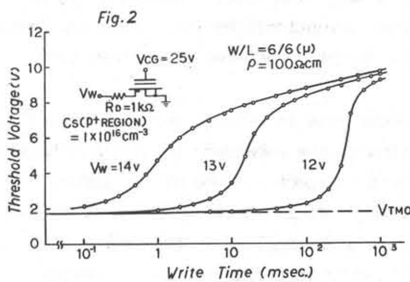
Conclusions Main features of the proposed memory transistor are summarized as follows.

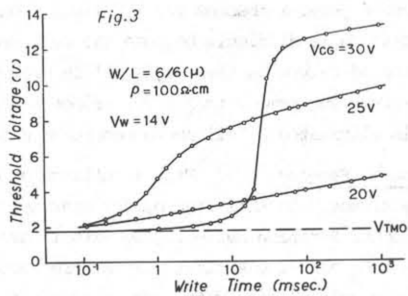
1) By the application of DSA technique, P^+-region with high surface concentration can be used not sacrificing high conductance of the memory transistor, and moreover the effective channel length can be determined irrespective of designed value, so the writing characteristics are much improved. In addition to that, the introduction of control and floating self-aligned gates' structure gurantees high integration and high performance of this memory transistor.

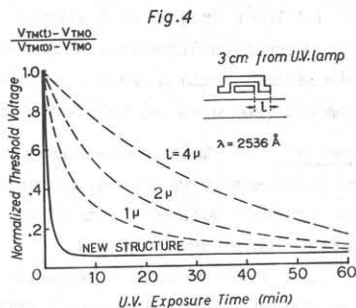
2) In the case of ultraviolet light erasure, the shielding effect of U.V by the control gate of second poly.Si can be prevented, so the erase characteristics of the proposed device are drastically improved compared to conventional ones.

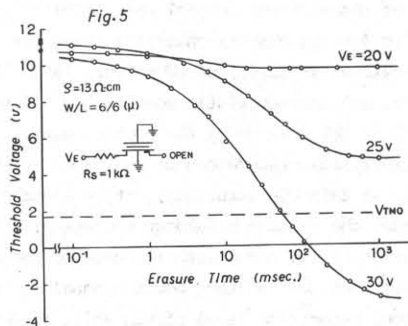
3) Combination of writing by channel electron injection and erasure by surface avalanche hole injection makes the realization of large capacity EEPROMs possible within the scheme of 1Tr/bit organization and positive applied voltages only.











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