A—5—1 "MFS FET" - A New Type of Nonvolatile Memory Switch Using PLZT Film

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Recently, a considerable amount of potential needs has been gathered on semiconductor nonvolatile memory elements from the viewpoints of high speed accessing, low power dissipation, high packing density and mass productivity. For this purpose, the controlling interface stored charge type field effect transistor, such as MNOS, MAOS and the floating metal gate FET, has been developed so far. Practical disadvantages to be solved in this kind of FET are high operating voltage for switching , existence of creeping effect of driving parameters and the degradation. Another type of semiconductor nonvolatile memory proposed is a ferroelectric field effect transistor - MFS(Metal Ferroelectric Semiconductor)FET- with a thin ferroelectric gate insulator. Since Moll and Tarui have demonstrated a conductivity modulation in the combination of CdS film on TGS crystal[1] , a series of experimental trials to make a good thin ferroelectric film has been done on various materials such as SbSI[2] , $Bi_4Ti_3O_{12}$[3] , PZBFN[4] and PLZT[5] . Among these materials PLZT has some advantages for the fabrication technology and device availability, that is, i) easy to control both ferroelectric and electrical properties by controlling the compositions and doped impurities ii) optical transparency of the material can be applicable to the opto-electronic functional element iii) having a possibility of the driving power reduction and so on.

We have conducted a systematic investigation on PLZT-PSZT ceramic system[6] and their thin film[7] . In this paper we describe a series of technical data on the MFS FET using PLZT thin film gate which might act as a programable nonvolatile memory switch having the low threshold voltage and IC capability.

A schematic diagram of the device construction and its operating principle are illustrated in Fig. 1. A step-like change in the interface built-in potential by controlling the ferroelectric polarization has been observed in the PLZT thin film on GaAs and Si single crystal heterostructure junction. There exists a clear clamping effect in the interface potential due to the ferroelectric hysteresis of PLZT. An RF sputtering method in the mixture gas of argon(90%)-oxygen(10%) with the pressure of $\sim 10^{-1}$ torr was used for the preparation of PLZT thin film. Well-reacted PLZT 18/0/100 powder was prepared as a target by the chemical preparation method.[8] The substrate temperature was varied in the range from room temperature(water-cooled substrate) up to 400°C. The deposition rate obtained under these conditions is in the range from 2000 to 4000 Å/hour with the RF power of 1.2~3 watts/cm^2, and the film thickness was ~1 μm. Most of the

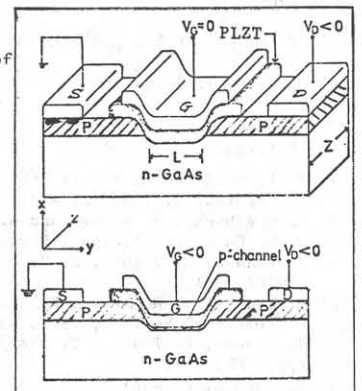

Fig.1 Schematic diagram of the MFS FET

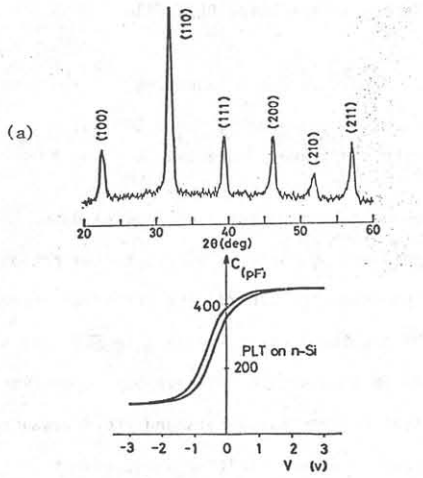

Fig.2 (a) X-ray diffraction pattern of PLZT thin film deposited on Si.
(b) C-V characteristics of the PLZT thin film on Si.

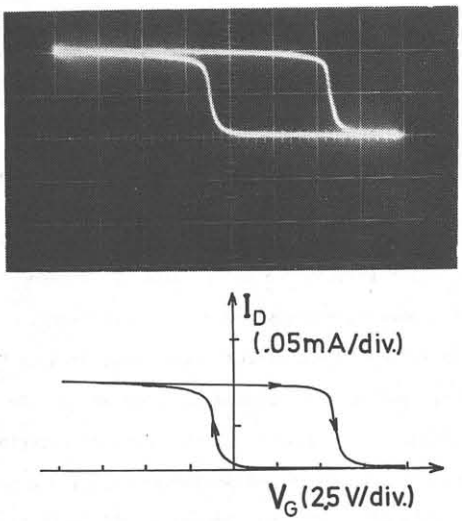

Fig.3 I_D-V_G characteristics of P-channel GaAs MFS-FET.

as-deposited films has non-crystalline or pyrochlore type structure and shows paraelectric characteristics. The perovskite type structure which usually indicates ferroelectric properties has been observed by heating the as-deposited film above 500°C for several hours. Fig. 2(a) shows X-ray diffraction pattern of PLZT thin film prepared by this method. C-V characteristics of the PLZT thin film on the Si single crystal is shown in Fig. 2(b). The details of preparation technology were almost same as that of our previous paper[5]. A typical result of the switching and memory hysteresis characteristics of the device is shown in Fig. 3. As can be seen from the figure, writing "0 to 1" threshold gate voltage is estimated to be about 1.5V and erasing "1 to 0" threshold gate voltage is ∿6V and drain current of "1" state is ∿1mA. Therefore flatband potential of this device is estimated to be about +3.75V for P-channel mode device. This operational performance obtained here is about one order smaller than that of $Bi_4Ti_3O_{12}$ gate MFS FET in the power level, that is the width of threshold gate voltage reported is ∿30V and on state current is 2.7mA in the $Bi_4Ti_3O_{12}$[3]. More informations of the technical data on the developed PLZT device will be introduced and discussed at the presentation.

References

1) J. L. Moll and Y. Tarui: IEEE Trans. ED-10 (1963) 338.
2) M. Yoshida, K. Yamanaka and Y. Hamakawa: Japan. J. Appl. Phys. 12 (1973) 1966.
3) K. Sugibuchi, Y. Kurogi and N. Endo: J. Appl. Phys. 46 (1975) 2877.
4) D. W. Charpman: J. Appl. Phys. 40 (1969) 2381.
5) K. Tanaka, Y. Higuma, K. Yokoyama, T. Nakagawa and Y. Hamakawa: Japan. J. Appl. Phys. 15 (1976) 1381.
6) K. Tanaka, Y. Hamakawa, K. Wakino, K. Minai and K. Ozawa: Trans. Electronic Component Professional Meeting, IECE, Japan CPM 73-85 (1973-11) in Japanese.
7) Y. Higuma, K. Tanaka, T. Nakagawa, T. Kariya and Y. Hamakawa: (to be published in Japan. J. Appl. Phys.).
8) M. Murata, K. Wakino, K. Tanaka and Y. Hamakawa: Materials Res. Bull. 11 (1976) 323.