A — 2 — 2 (Invited) Non-thermal Carrier Generation in MOS Structures

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Efforts to increase device packing density and to improve device performance in MOS LSI's, are focused on shorter channel length, thinner gate oxide and shallower junction depth. If device dimensions are reduced while maintaining operating voltages, hot carrier phenomena can occur in the increased electric field, which result in device instability or failure operation. Radiation effects also cause similar instability, or failure known as "soft errors". In this paper we describe the influence of non-thermal carrier generation, and present a series of experiments and phenomenological models.

When an n-channel MOSFET is turned on, the electrons flow from the source to the drain, and gain kinetic energy from the electric field. If they exceed impact ionization threshold, electron-hole pairs can be generated. Most of the generated electrons flow to the drain, and the holes flow towards the substrate appearing as substrate current. However, some of the hot electrons having energies greater than the potential barrier at the $Si-SiO_2$ interface can be injected into the oxide (Fig.1). A small fraction of the injected electrons are trapped in the gate oxide, resulting in a threshold voltage shift and/or transconductance degradation[1]. Both experimental results and theoretical modeling of two-dimentional transport have been reported, however, the major difficulties are within the measurement of the gate current in pre-avalanche condition, which is extremely low level for typical size devices.

A stacking gate MOS structure is successfully used to measure the electronic gate currents of 10^{-13} to 10^{-20} amps per one micron of device width biased in the normal or slightly stressed operating conditions. The injected electrons are stored in the floating gate, therefore, the gate current is effectively integrated resulting in threshold voltage shift. Fig.2 shows results of the gate and the substrate currents measurement, which gives absolute emission probability. Comparing with the threshold voltage shift of single level MOSFET, the effective trapping efficiency, about 5×10^{-3}, was also given.

The substrate current, which is the result of the hole flow, has influence on the device characteristics through the effective substrate voltage modulation[2]. The substrate current can even forward-bias the source junction, then electrons are injected into the substrate and thus activate the parasitic bipolar transistor. Finally breakdown of the device will occur when the drain bias reaches BV_{CEO}[3]. Substrate current was culculated by two-dimensional analysis of both the electric field and the current distributions. The culculated results showed good agreement with the measured substrate current. Fig.3 shows typical substrate current vs. applied gate voltage characteristics for 1μm and 2μm effective channel length NMOS transistors.

In spite of the high retarding electric field towards the substrate, electron injection in substrate has been observed directly by charge-coupled device measurement[4]. The fact can be explained by a secondary impact ionization by accelerated hole flow in the depletion region towards the substrate. As in the first impact ionization by the channel hot electron, the holes flow to the substrate and the electrons flow into the drain. However, some electrons which

are generated near the depletion edge can reach the neutral region and then diffuse in the bulk (Fig.1; 1V). Fig.4 shows the result of the spatial distribution measurement of the injected electronic current in the substrate. The effective diffusion length of the excess electrons obtained from Fig.4 was about 60μm, which reasonably corresponds to the reported value. Holding time degradation due to the electrically generated excess electrons has also been observed in a 16-kbit dynamic MOS RAM[5] and also with test devices.

Other design constraint than those relating to the thermally generated leakage current, will be discussed, putting emphasis on the electrical carrier generation and the radiation effects.

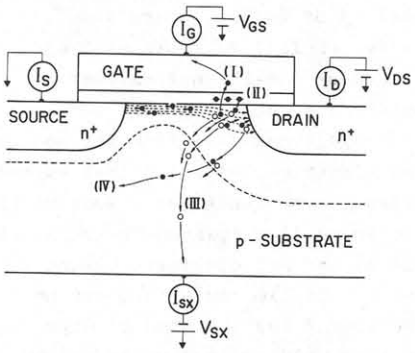

Fig.1 A schematic diagram of a NMOS transistor illustrating the primary and the secondary carrier generations by channel hot electrons.

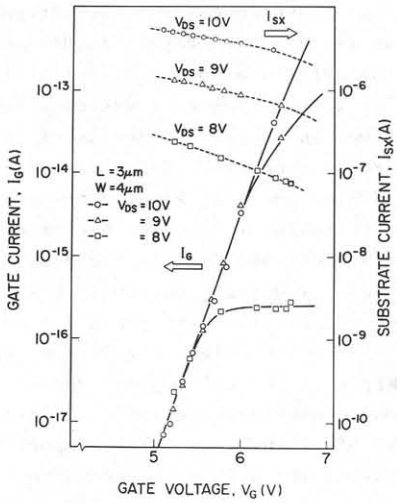

Fig.2 Electronic gate current and Substrate current vs. gate voltage in pre-avalanche region for various drain voltages.

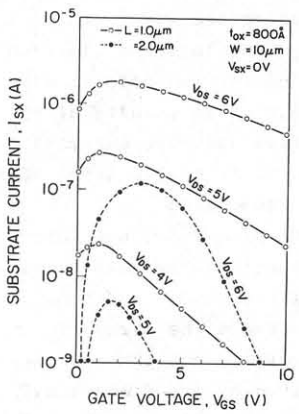

Fig.3 Substrate current vs. gate voltage of NMOS transistors with 1μm and 2μm channel lengths.

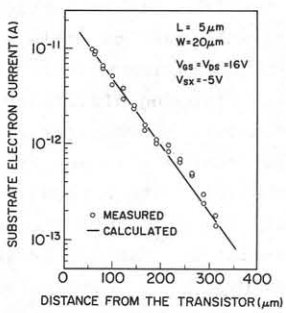

Fig.4 Electronic current distribution in the substrate for the distance from the source transistor.

1) T.H.Ning, C.M.Osburn, and H.N.Yu, J. Electron. Materials, vol.6, 65-76 (1977).

2) T.Toyabe, K.Yamaguchi, S.Asai, and M.S.Mock, IEEE Trans. Electron Devices. vol. ED-25, 825-832 (1978).

3) E.Sun, J.Moll, J.Berger, and B.Alders, IEDM Tech. Digest, 478-482 (1978).

4) J.Matsunaga, and S.Kohyama, Appl. Phys. Lett., vol.33, 335-337 (1978).

5) J.Matsunaga, R.Furuyama, and S.Kohyama, Proc. 15th Symp. on Semicond. and IC Tech., 132-137 (1978) (in Japanese).